A Multilevel Inverter with Streamlined Components and Reduced THD using the Multicarrier Sine PWM Approach for Resistive and Inductive Loads

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***Abstract*—This paper explores the design journey of a ground-breaking 129-level inverter, where innovation and fantasy collide, in the fascinating field of power electronics. This inverter, which embraces the mystique of having fewer components and goes beyond harmonic norms, is a paradigm change in multilevel converter technology. The trip starts with an innovative method that deliberately reduces parts and toggles, defying the common assumption that higher levels require more complexity. The result is a captivating symphony of voltage steps that elegantly rise to 129 levels while simultaneously lowering the Total Harmonic Distortion (THD). The waveform of the inverter mimics a sine wave with unparalleled fidelity, akin to a mystical incantation. A careful control strategy that smoothly switches by multicarrier Pulse Width Modulation (PWM) technology underpins this amazing performance. In addition to reducing THD, the control mechanism fully utilizes the inverter's fewer components. This paper reveals not just an inverter but also an enchanted object that transcends traditional bounds as it invites readers to explore the fantasy world of power electronics. This 129-level marvel invites scientists, engineers, and dreamers to set out on an adventure, stretching the bounds of what is conceivable in the magical field of power conversion.**

***Index Terms*— Control strategy, Harmonic reduction, Multilevel inverter, Power electronics, Pulse Width Modulation (PWM), 129-level inverter, Streamlined components, Total Harmonic Distortion (THD).**

I. INTRODUCTION

The search for creative and effective multilevel inverters in the rapidly changing field of power electronics has produced a remarkable achievement: a 129-level inverter that pushes the limits of harmonic suppression [1]. With power conversion systems becoming more and more essential to our technological environment, there is an increasing need for inverters that can generate clean, sinusoidal outputs with low Total Harmonic Distortion (THD). The simultaneous requirement for simplicity, efficiency, and adaptability across a range of load types intensifies this task even further [2] [3] [4] [5] [6] .

Our innovation is centered on the thoughtful combination of cutting-edge control methods and efficient circuit design. The Multicarrier Sine Pulse Width Modulation (PWM) approach emerges as the harmonic harmony orchestrator at the heart of this design. Multicarrier Sine PWM, guarantees a smoother transition between voltage levels, enabling sinewave outputs that closely resemble the perfect waveform. This control approach turns out to be crucial for obtaining strong performance and remarkable THD reduction [7] [8] [9] [10] .

The scope of this accomplishment extends beyond theoretical models. After a thorough modeling exercise, the inverter shows off its capabilities by generating outputs that are precisely sinewaves with low THD. Validations from experiments act as the furnace in which theory is switched into concrete reality. The inverter not only maintains its promise of harmonic harmony but does so with an efficiency and elegance that beyond conventional expectations, having been carefully tested under both resistive and inductive load circumstances.
The simple architecture and control technique used to build this 129-level inverter are explained in this study. By exploring the subtleties of its design, we pave the way for an exciting voyage into the realm of power electronics in the future, where sophistication and simplicity come together to create a paradigm-shifting change in multilevel inverter technology.

II. A BRIEF ANALYSIS OF EXISTING MLI TOPOLOGIES

Following the completion of the literature review [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], it is evident that the authors attempted to build the multilevel inverter using less capacitors, diodes, circuits for gate drivers, switches, and sources of DC supply. Just a few of them did not focus on THD reduction, while others attempted to lower THD as well. They have employed a variety of control approaches and topologies to accomplish these goals. The table below displays different topologies created in different years by different authors. The quantity of voltage levels at output, semiconductor switches (the number of circuits for gate drivers equals the quantity of switches), sources of DC supply, capacitors, and diodes utilized in a few of the current topologies are all examined. Analysis Table 1 tells us that many semiconductor switching devices, sources of DC supply, capacitors, and diodes were used to

obtain the multilevel output voltages.

A large range of devices have been employed by most authors, even for low output voltage levels. The aforementioned components increase in number as the level of output voltage increases. So that the circuit and control may not become overly sophisticated, the researchers are attempting to build straightforward, economical, and efficient topologies with straightforward control approaches [31]. Due to the high industrial productivity of multilevel inverter implementation, academics and industrial people are working to find the simplest and most efficient ways to improve the multilevel inverter design and control. The count of components utilized in various references from the literature review and the suggested strategy are shown in the table I.

TABLE I
COMPARISON WITH THE EXISTING TOPOLOGIES

Ref	No. of levels	No. of Switches	No. of DC sources	No. of Capacitors	No. of Diodes	THD%
1	53	14	3	0	0	1.42
2	15	7	3	0	3	10.03
3	7	14	1	3	0	19.86
4	15	10	3	0	0	3.18
5	13	9	2	2	3	0.12
6	13	9	2	4	0	7.1
7	7	8	1	2	1	18.28
8	9	11	1	3	0	14.1
9	21	10	3	0	0	3.49
10	9	10	2	2	0	5.15
11	71	28	13	0	0	1.14
12	13	14	1	3	1	5.27
13	17	12	1	3	2	6.9
14	17	14	4	4	0	4.23
15	31	10	4	0	0	3.62
16	25	10	2	4	0	3.25
17	17	9	2	4	0	4.79
18	31	10	3	0	0	3.32
19	41	14	8	0	0	1.992
20	15	10	3	0	0	3.18
Pro	129	10	7	0	6	1.32

III. Proposed 129 Level Inverter Topology

In this proposed topology, six switches and seven DC sources (i.e) six DC sources, one DC source per switch, and one additional switch at the top of the topology are employed to obtain the 129 level inverter. In addition, the series combination of switches and sources of DC supply is linked in parallel to the six clamping diodes. An H-bridge serves as a polarity generator to generate the polarities for the AC sinewave. LCL filter is used to further minimize harmonics. The 129-level plan that has been suggested is seen in fig 1.

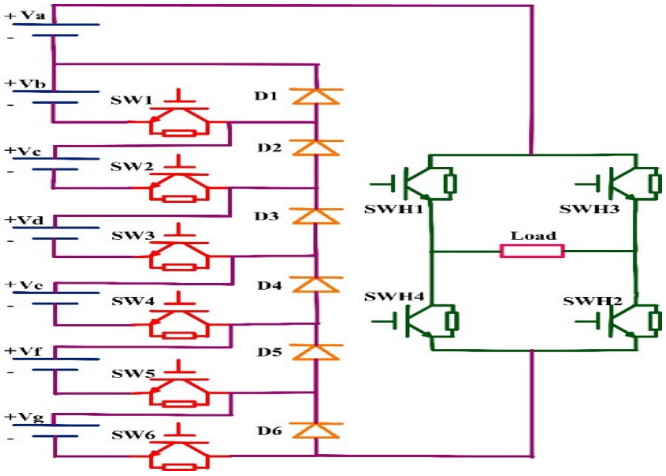

Fig. 1. A 129-level inverter topology proposal

This topology's DC sources are arranged in the ratio 1:1:2:4:8:16:32 as binary weighted. The set DC voltage algorithm is:

Vdc=5V, Va= 1Vdc=5V, Vb= 1Vdc=5V, Vc= 2Vdc= 10V, Vd= 4Vdc=20V, Ve= 8Vdc=40V, Vf= 16Vdc=80V, Vg= 32Vdc=160V.

A. *Modes of Operation*

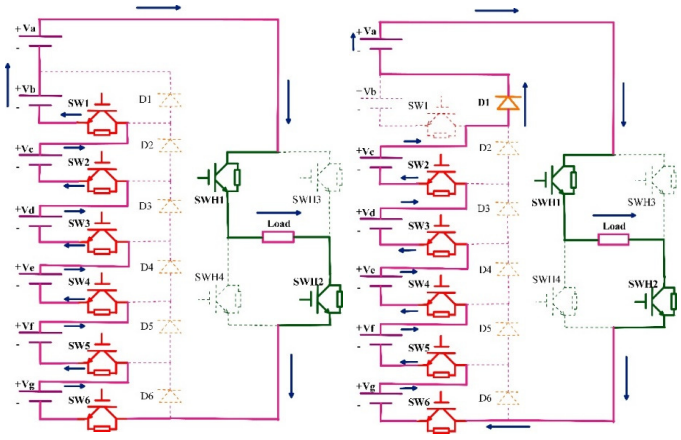

Fig. 2. Mode1 & 2 of a proposed 129 level Inverter Topology

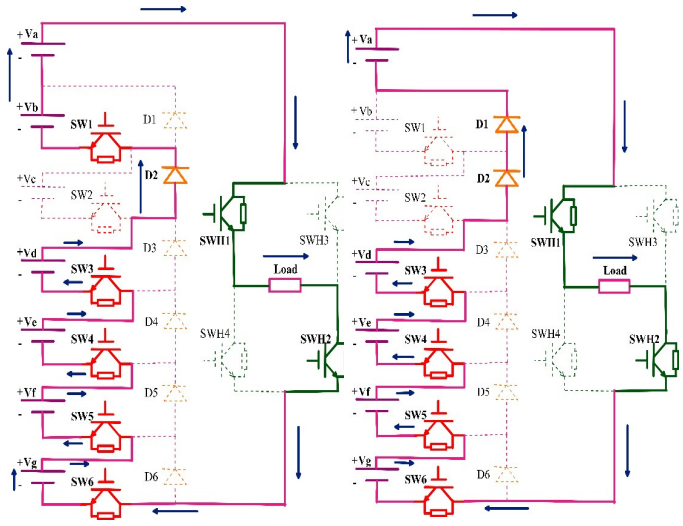

Fig. 3. Mode3 & 4 of a proposed 129 level Inverter Topology.

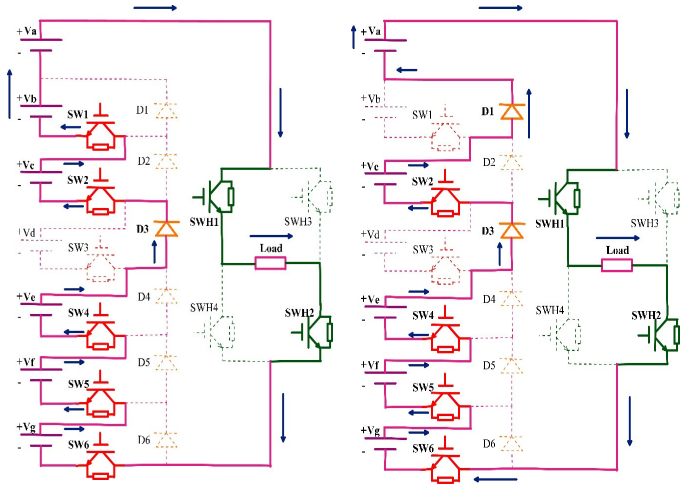

Fig. 4. Mode5 &6 of a proposed 129 level Inverter Topology.

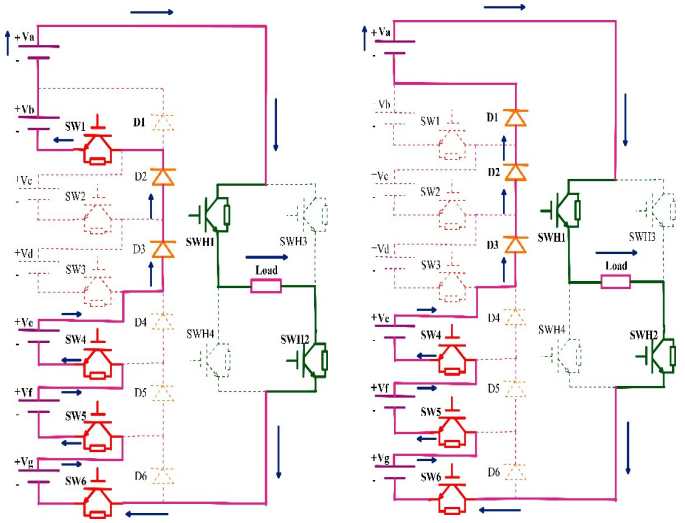

Fig. 5. Mode7 &8 of a proposed 129 level Inverter Topology

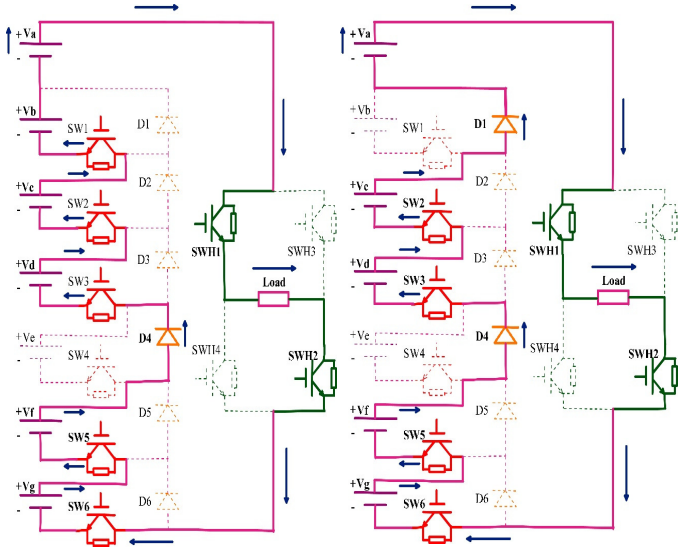

Fig. 6. Mode9 &10 of a proposed 129 level Inverter Topology

The different modes of operation are given below using colorful circuit diagrams with the proper indication of current flow for ON and OFF conditions of the specified switches. There are 129 modes of operation. Sixty four negative voltage values and sixty four positive voltage levels in total are obtained.

The switches SW_{H1} and SW_{H2} pair are switched on for all positive polarity values, and the switches SW_{H3} and SW_{H4} pair are made on for all values of negative polarity. The voltage output is "zero" when all the switches and diodes are off, regardless of how the H-bridge switch pairs are turned on or off. For the simplicity, 10 modes of operation are displayed in pictorial form in fig.2, 3, 4, 5 and 6. The switching modes are tabulated as in table II.

TABLE II
SWITCHING MODES

SW_1	SW_2	SW_3	SW_4	SW_5	SW_6	Voltage output V_0 (V)
ON	ON	ON	ON	ON	ON	+/-320
OFF	ON	ON	ON	ON	ON	+/-315
ON	OFF	ON	ON	ON	ON	+/-310
OFF	OFF	ON	ON	ON	ON	+/-305
ON	ON	OFF	ON	ON	ON	+/-300
OFF	ON	OFF	ON	ON	ON	+/-295
ON	OFF	OFF	ON	ON	ON	+/-290
OFF	OFF	OFF	ON	ON	ON	+/-285
ON	ON	ON	OFF	ON	ON	+/-280
OFF	ON	ON	OFF	ON	ON	+/-275
ON	OFF	ON	OFF	ON	ON	+/-270
OFF	OFF	ON	OFF	ON	ON	+/-265
ON	ON	OFF	OFF	ON	ON	+/-260
OFF	ON	OFF	OFF	ON	ON	+/-255
ON	OFF	OFF	OFF	ON	ON	+/-250
OFF	OFF	OFF	OFF	ON	ON	+/-245
ON	ON	ON	ON	OFF	ON	+/-240
OFF	ON	ON	ON	OFF	ON	+/-235
ON	OFF	ON	ON	OFF	ON	+/-230
OFF	OFF	ON	ON	OFF	ON	+/-225
ON	ON	OFF	ON	OFF	ON	+/-220
OFF	ON	OFF	ON	OFF	ON	+/-215
ON	OFF	OFF	ON	OFF	ON	+/-210

OFF	OFF	OFF	ON	OFF	ON	+/-205
ON	ON	ON	OFF	OFF	ON	+/-200
OFF	ON	ON	OFF	OFF	ON	+/-195
ON	OFF	ON	OFF	OFF	ON	+/-190
OFF	OFF	ON	OFF	OFF	ON	+/-185
ON	ON	OFF	OFF	OFF	ON	+/-180
OFF	ON	OFF	OFF	OFF	ON	+/-175
ON	OFF	OFF	OFF	OFF	ON	+/-170
OFF	OFF	OFF	OFF	OFF	ON	+/-165
ON	ON	ON	ON	ON	OFF	+/-160
OFF	ON	ON	ON	ON	OFF	+/-155
ON	OFF	ON	ON	ON	OFF	+/-150
OFF	OFF	ON	ON	ON	OFF	+/-145
ON	ON	OFF	ON	ON	OFF	+/-140
OFF	ON	OFF	ON	ON	OFF	+/-135
ON	OFF	OFF	ON	ON	OFF	+/-130
OFF	OFF	OFF	ON	ON	OFF	+/-125
ON	ON	ON	OFF	ON	OFF	+/-120
OFF	ON	ON	OFF	ON	OFF	+/-115
ON	OFF	ON	OFF	ON	OFF	+/-110
OFF	OFF	ON	OFF	ON	OFF	+/-105
ON	ON	OFF	OFF	ON	OFF	+/-100
OFF	ON	OFF	OFF	ON	OFF	+/-95
ON	OFF	OFF	OFF	ON	OFF	+/-90
OFF	OFF	OFF	OFF	ON	OFF	+/-85
ON	ON	ON	ON	OFF	OFF	+/-80
OFF	ON	ON	ON	OFF	OFF	+/-75
ON	OFF	ON	ON	OFF	OFF	+/-70
OFF	OFF	ON	ON	OFF	OFF	+/-65
ON	ON	OFF	ON	OFF	OFF	+/-60
OFF	ON	OFF	ON	OFF	OFF	+/-55
ON	OFF	OFF	ON	OFF	OFF	+/-50
OFF	OFF	OFF	ON	OFF	OFF	+/-45
ON	ON	ON	OFF	OFF	OFF	+/-40
OFF	ON	ON	OFF	OFF	OFF	+/-35
ON	OFF	ON	OFF	OFF	OFF	+/-30
OFF	OFF	ON	OFF	OFF	OFF	+/-25
ON	ON	OFF	OFF	OFF	OFF	+/-20
OFF	ON	OFF	OFF	OFF	OFF	+/-15
ON	OFF	OFF	OFF	OFF	OFF	+/-10
OFF	OFF	OFF	OFF	OFF	OFF	+/-05
OFF	OFF	OFF	OFF	OFF	OFF	+/-0

The following is an explanation of the switching combinations:

The diode linked in parallel with a switch that's plugged into a DC source is turned off when the switch is made ON because the current prefers to flow via the switch rather than the diode. The voltage output is accompanied with the particular source of DC voltage that is associated with the ON switch. When a switch is off, the source voltage that corresponds to the switch is removed from the output and the current is bypassed through the diode that is connected in parallel to the switch. Using this basic technique, 320V is the voltage output obtained by turning on all of the switches, SW_1 through SW_6. The diode D_1 turns on and the output voltage is 315V when switches SW_2 through SW_6 are switched on and SW_1 is switched off. D_2 turns on and the output voltage is 310V while SW_2 is off and every other switch is on. The voltage output is 305V when SW_1 and SW_2 are switched off, turning on D_1 and D_2. D_3 turns on and the output voltage is 300V while SW_3 is off. D_1 and D_3 turn on when SW_1 and SW_3 are switched off, producing a voltage output of 295V. D2 and D3 turn on when SW_2 and SW_3 are switched off, producing an output voltage of 290V. D_1, D_2, and D_3 turn on when SW_1, SW_2, and SW_3 are switched off, generating an output voltage of 285V. D_4 turns on and the output voltage is 280V when SW_4 is switched off. D_1 and D_4 turn on when SW_1 and SW_4 are switched off, delivering an output voltage of 275V. D_2 and D_4 turn on when SW_2 and SW_4 are switched off, giving an output voltage of 270V. D_1, D_2, and D_4 turn on when SW_1, SW_2, and SW_4 are made off, generating an output voltage of 265V. D_3 and D_4 are on when SW_3 and SW_4 are switched off, providing an output voltage of 260V. D_1, D_3, and D_4 turn on when SW_1, SW_3, and SW_4 are made off, and the voltage output is 255V. The voltage output is 250V when SW_2, SW_3, and SW4 are switched off and D_2, D_3, and D_4 turn on. The output voltage is 245V when SW_1, SW_2, SW_3, and SW_4 are switched off and D_1, D_2, D_3, and D_4 turn on. D_5 turns ON and the output voltage is 240V when SW_5 is switched off. D_1 and D_5 turn on when SW_1 and SW_5 are switched off, giving an output voltage of 235V. D_2 and D_5 turn on when SW_2 and SW_5 are switched off, leading to an output voltage of 230V. D_1, D_2, and D_5 turn on when SW_1, SW_2, and SW_5 are switched off, bringing about an output voltage of 225V. D_3 and D_5 turn on when SW_3 and SW_5 are switched off, culminating in a 220V output voltage. D_1, D_3, and D_5 turn on when SW_1, SW_3, and SW_5 are switched off, causing an output voltage of 215V. D_2, D_3, and D_5 turn on when SW_2, SW_3, and SW_5 are switched off, yielding an output voltage of 210V. The output voltage is 205V when SW_1, SW_2, SW_3, and SW_5 are switched off. D_1, D_2, D_3, and D_5 turn ON. D_4 and D_5 turn ON when SW_4 and SW_5 are switched off, producing an output voltage of 200V. D_1, D_4, and D_5 turn on when SW_1, SW_4, and SW_5 are switched off, causing an output voltage of 195V. D_2, D_4, and D_5 turn on when SW_2, SW_4, and SW_5 are switched off, yielding an output voltage of 190V. The output voltage is 185V when SW_1, SW_2, SW_4, and SW_5 are made off and D_1, D_2, D_4, and D_5 turn ON. D_3, D_4, and D_5 turn on when SW_3, SW_4, and SW_5 are switched off, generating an output voltage of 180V. The output voltage is 175V when SW_1, SW_3, SW_4, and SW_5 are turned off and D_1, D_3, D_4, and D_5 turn on. The output voltage is 170V when SW_2, SW_3, SW_4, and SW_5 are switched off and D_2, D_3, D_4, and D_5 turn on. D_1 through D_5 are on and the output voltage is 165V when SW_1 through SW_5 are off and only SW_6 is on. D_6 turns on and the output voltage is 160V when SW_1 through SW_5 are all on and only SW_6 is off. D_1 and D_6 turn on when SW_1 and SW_6 are off, resulting in an output voltage of 155V. The output voltage is 150V when D_2 through D_6 are on and SW_2 to SW_6 are off. D_1, D_2, and D_6 turn on when SW_1, SW_2, and SW_6 are switched off, delivering an output voltage of 145V. D_3 and D_6 turn on when SW_3 and SW_6 are off, creating an output voltage of 140V. D_1, D_3, and D_6 turn on when SW_1, SW_3, and SW_6 are switched off, developing an output voltage of 135V. D_2, D_3, and D_6 turn on when SW_2, SW_3, and SW_6 are switched off, leading an output voltage of 130V. The output voltage is 125V when SW_1, SW_2, SW_3, and SW_6 are switched off and D_1, D_2, D_3, and D_6 turn on. D_4 and D_6 turn ON when SW_4 and SW_6 are switched off, effecting a 120V output voltage. D_1, D_4, and D_6 turn on when SW_1, SW_4, and SW_6 are switched off, producing an output voltage of 115V. D_2, D_4, and D_6 turn on when SW_2, SW_4, and SW_6 are switched off, resulting in an output voltage of 110V. The output voltage is 105V when SW_1, SW_2, SW_4, and SW_6 are switched off and D_1, D_2, D_4, and D_6 turn on. D_3, D_4,

and D_6 turn on when SW_3, SW_4, and SW_6 are switched off, resulting in an output voltage of 100V. The output voltage is 95V when SW_1, SW_3, SW_4, and SW_6 are switched off and D_1, D_3, D_4, and D_6 turn on. The output voltage is 90V when SW_2, SW_3, SW_4, and SW_6 are switched off and D_2, D_3, D_4, and D_6 turn on. The output voltage is 85V when SW_5 is the only switch that is on and all other switches are off, with the exception of D_5. D_5 and D_6 turn on when SW_5 and SW_6 are switched off, resulting in an output voltage of 80V. D_1, D_5, and D_6 turn on and the output voltage is 75V when SW_1, SW_5, and SW_6 are made off. D_2, D_5, and D_6 turn on when SW_2, SW_5, and SW_6 are switched off, resulting in an output voltage of 70V. The output voltage is 65V when SW_1, SW_2, SW_5, and SW_6 are switched off and D_1, D_2, D_5, and D_6 turn ON. D_3, D_5, and D_6 turn on and the output voltage is 60V when SW_3, SW_5, and SW_6 are switched off. The output voltage is 55V when SW_1, SW_3, SW_5, and SW_6 are made off and D_1, D_3, D_5, and D_6 turn on. The output voltage is 50V and D_2, D_3, D_5, and D_6 turn on when SW_2, SW_3, SW_5, and SW_6 are switched off. With the exception of D_4, all other diodes turn on when SW_4 is the only switch that is on, resulting in an output voltage of 45V. D_4, D_5, and D_6 turn on and the output voltage is 40V when SW_4, SW_5, and SW_6 are made off. D_1, D_4, D_5, and D_6 turn on and the output voltage is 35V while SW_1, SW_4, SW_5, and SW_6 are turned off. The output voltage is 30V when SW_2, SW_4, SW_5, and SW_6 are switched off, while D_2, D_4, D_5, and D_6 turn on. The output voltage is 25V when SW_3 is the only switch that is ON and all other switches are off, with the exception of D_3. D_1 and D_2 are off and every other diode is on while SW_1 and SW_2 are on and every other switch is off. Right now, the voltage output is 20V. The voltage output is 15V when SW_2 is the only switch that is on and all other switches are off. All other diodes become ON except D_2. The output voltage is 10V when SW_1 is the only switch that is ON and all other switches are off, with the exception of D_1. The output voltage is 5V when all switches are off and all diodes are on. Therefore, the output consists of 129 voltage levels in total, comprising zero, positive 64, and negative 64 levels. This topology yields a higher number of step levels at the output, which results in a waveform that is very near to a sinewave with a very low THD. The DC link voltage has 65 positive voltage levels. This DC voltage is converted into 129 level AC output using an H- bridge.

B. Modulation Strategy

Use By measuring the amplitude of each harmonic frequency in the output waveform and computing the ratio of the sum of the squares of the harmonic amplitudes to the square of the fundamental frequency amplitude, the total harmonic distortion (THD) for a multilevel inverter can be obtained. Because a multilevel inverter's output waveform has many voltage levels, calculating THD for one can be a little trickier than for a traditional two-level inverter. One popular technique is to break down the output waveform into its constituent harmonic components using Fourier series analysis, and then, the calculation given below can be used to determine the total harmonic distortion (THD) [32], [33] .

$$THD = \sqrt{\frac{\sum_{n=2}^{N} V_n^2}{V_1^2}} \quad (1)$$

N is the overall quantity of harmonics that the summing takes into account.

The term "V_n" refers to the amplitude of the n^{th} harmonic in the output voltage or current's Fourier series representation.

V_1 denotes the signal's fundamental component.

To find the fundamental and various order harmonics of a signal, a Fourier analysis must be done:

Sine and cosine are used to express periodic signals [34].

$$F(x)= \frac{a_0}{2} + \sum_{n=1}^{\infty}[a_n \cos(nx) + b_n \sin(nx)] \quad (2)$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t)\cos(nt)\,dt, n \geq 0$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t)\sin(nt)\,dt, n \geq 1$$

This formula determines the THD as a percentage and gives an indication of the harmonic distortion in the signal. In actual use, the THD is frequently stated as a percentage of the signal's primary frequency component. More harmonics in the summation yield a more accurate depiction of the distortion. The harmonics are derived from the Fourier series analysis of the waveform.

First, the 129 level inverter scheme employs the multicarrier PWM technique while using filter. The basic equation for Multicarrier Pulse Width Modulation (PWM) is generally written in terms of the reference waveform and carrier signals. Here the Sine PWM method (SPWM) is used. To create the PWM waveform in SPWM, the reference waveform is compared to several carrier signals.

The equation for the PWM signal s (t) can be given as [8]:

$$S(t) = \frac{1}{2} + \frac{1}{2}\sin(2\pi f_c t) \quad (3)$$

Where f_c= frequency of the carrier signal

Several carrier signals with various frequencies are frequently employed in multicarrier PWM systems, and the reference waveform is compared with each carrier to produce the final PWM waveform [10].

IV. Results and Discussions

The simulation and experimental validation of a new 129-level inverter are done in this section. With fewer components and a lower Total Harmonic Distortion (THD), the inverter with a Multicarrier Sine Pulse Width Modulation (PWM) control method exhibits outstanding design. When compared to traditional counterparts, the proposed inverter exhibits greater THD reduction during the simulation phase, producing sine wave outputs for both resistive and inductive loads. 320V and 32A of output voltage and current are attained. The simulated circuit diagram is shown in Fig. 7. Fig. 8, 9 and 10 display the gate signals required to trigger the switches. The 65 level DC link voltage, voltage output and current are shown in fig. 11, 12 and 13. Fig. 14 illustrates how the voltage output and current output waveforms in a resistive load are remarkably distinct and in phase with one another. Fig. 15 illustrates how the output current of an inductive load lags the voltage. Fig. 16 and 17 represent the percentage THD of the voltage output for resistive and inductive loads as 1.32% and 2.26%, respectively. Simulation results and real hardware results agree well,

demonstrating the inverter's ability to produce clean sinewave under a resistive and inductive load scenarios. When compared to twenty reference papers given in table I that represent the cutting edge of multilevel inverter technology, the suggested 129-level inverter emerges as the winner of this thorough comparison examination. Critical metrics such as the number of step levels, switching devices, sources of DC supply, capacitors, diodes and total harmonic distortion (THD %), are all included in the comparison. The suggested inverter performs better than its competitors in terms of its improved harmonic control and reduced component count. Graphical representations clearly show the comparing patterns, highlighting the 129-level inverter design's effectiveness and grace. The confluence of hardware and simulation results signals a paradigm shift in multilevel inverter technology, where simplicity and creativity work together to rewrite the rules for efficiency and ease of use in power electronics.

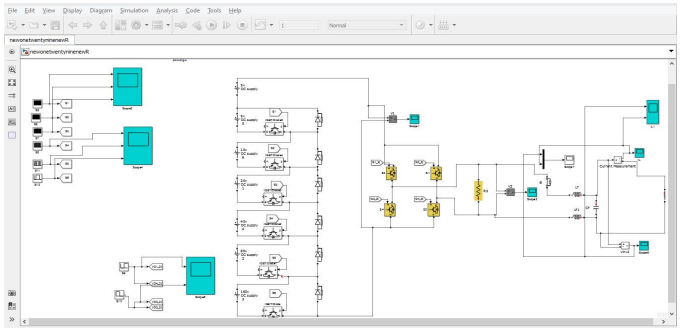

Fig.8 Circuit of the proposed scheme

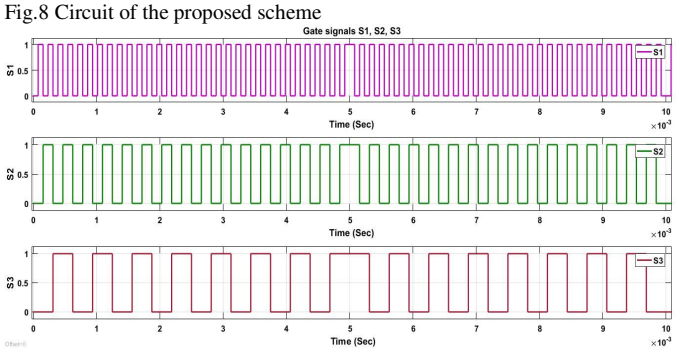

Fig. 9 Gate signals S1- S3

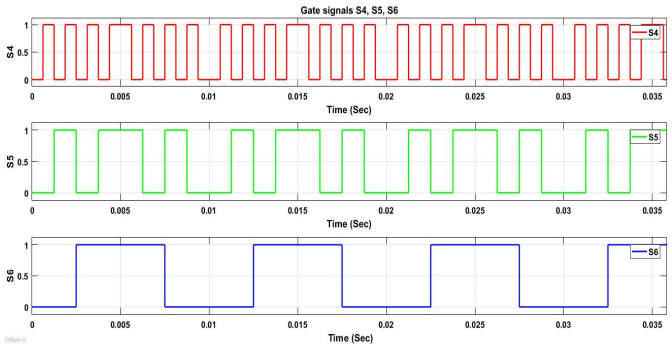

Fig. 10 Gate signals S4- S6

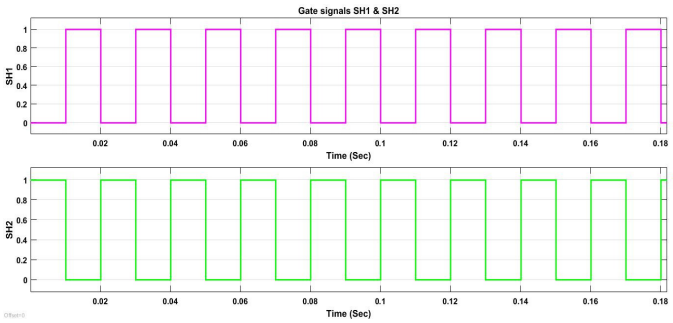

Fig. 11 Gate signals SH1 & SH2

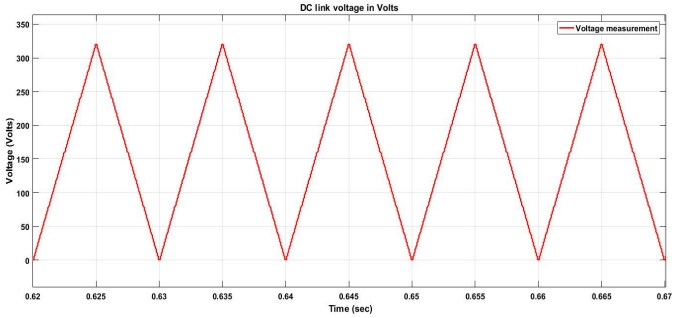

Fig. 12 65 levels of DC link voltage

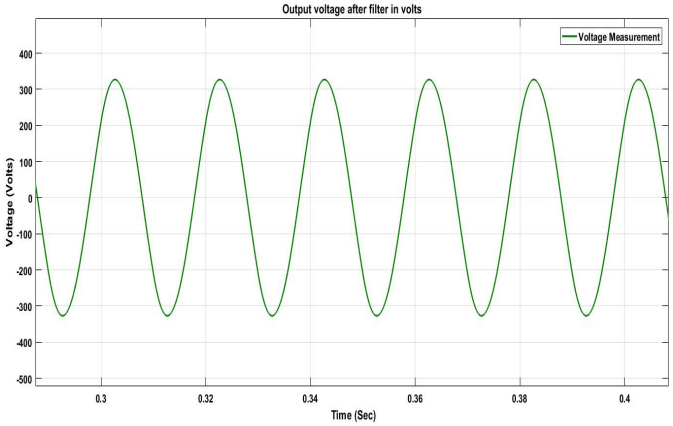

Fig. 13 The suggested 129 level inverter scheme's output voltage

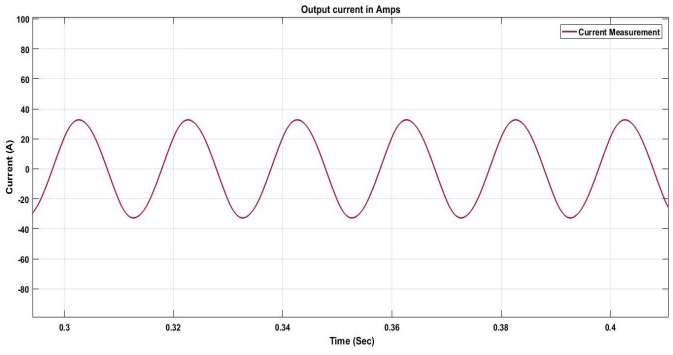

Fig. 14 The suggested 129-level inverter scheme's output current

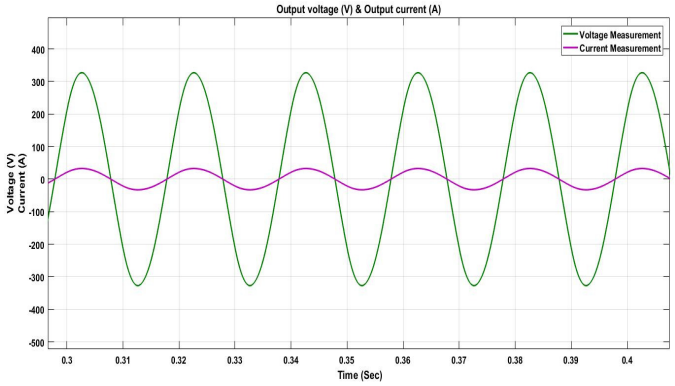

Fig. 15 129 levels of voltage and current outputs for an R load

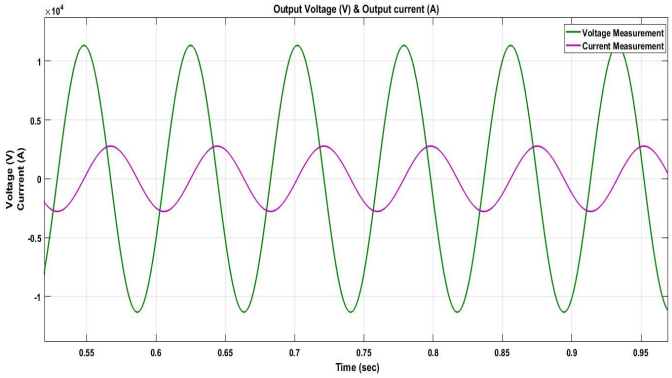

Fig. 16 129 levels of voltage and current outputs for an L load

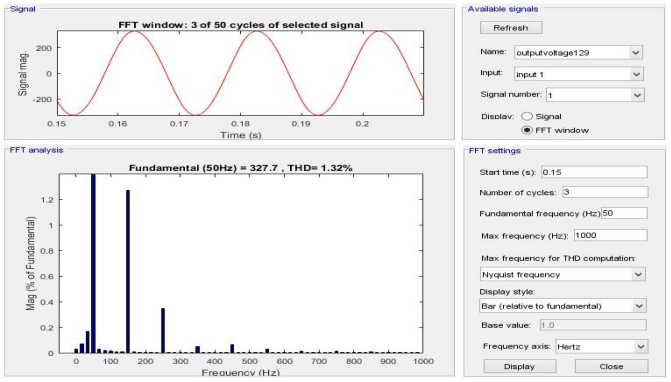

Fig. 17 THD of the R load's voltage output

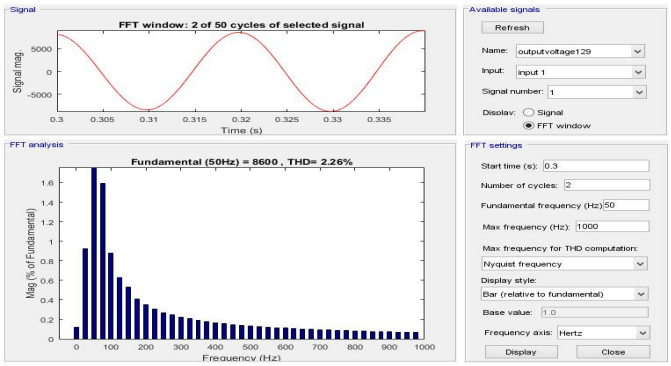

Fig. 18 THD of the L load's voltage output

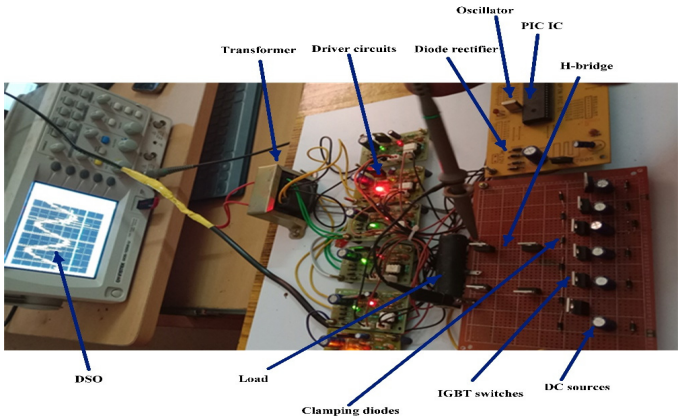

Fig. 19 Experimental set up of a 129 level inverter

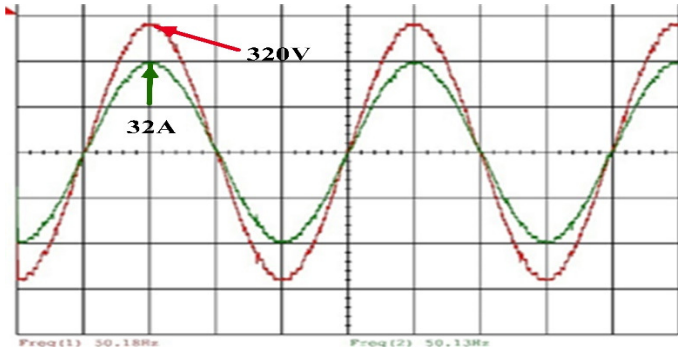

Fig. 20 A 129 level inverter's hardware voltage and current outputs for an R load

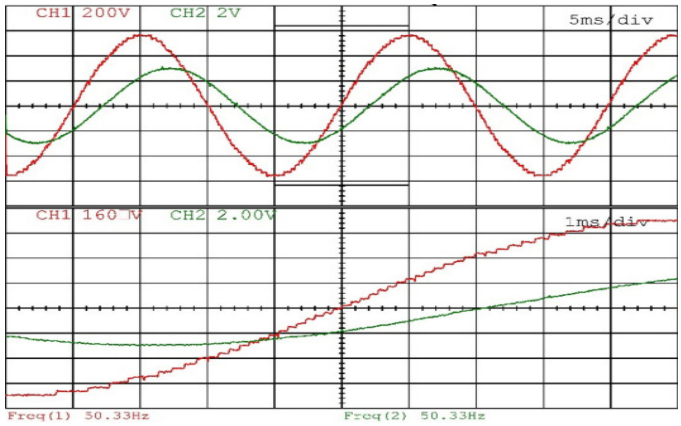

Fig. 21 A 129 level inverter's hardware voltage and current outputs for an L load

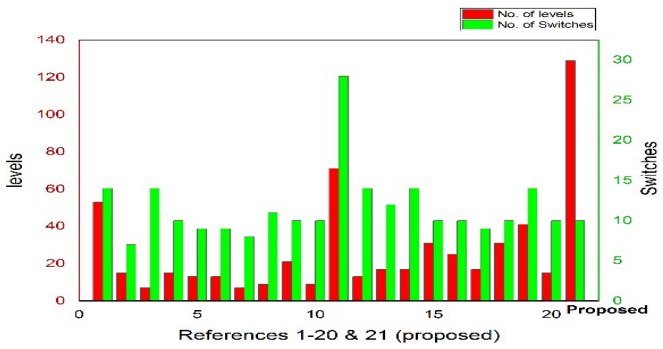

Fig. 22 No. of levels& Switches

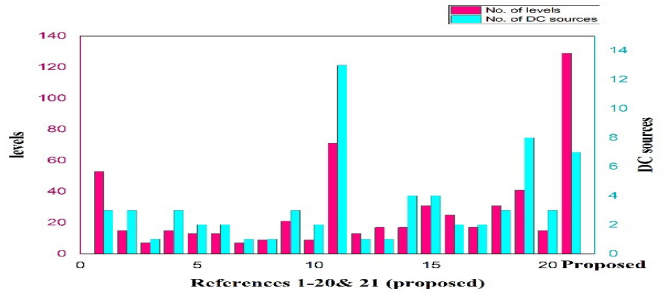

Fig. 23 No. of levels& DC sources

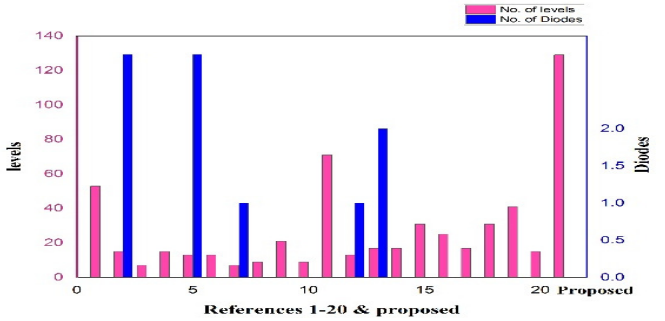

Fig. 24 No. of levels& Capacitors

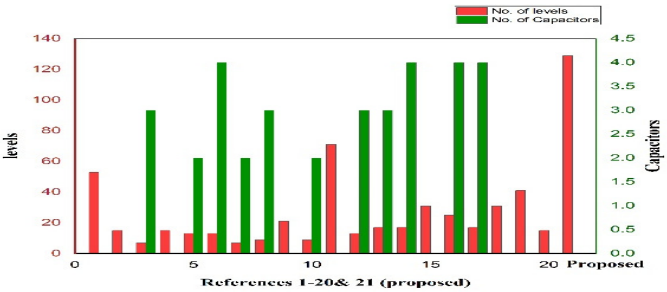

Fig. 25 No. of levels& Diodes

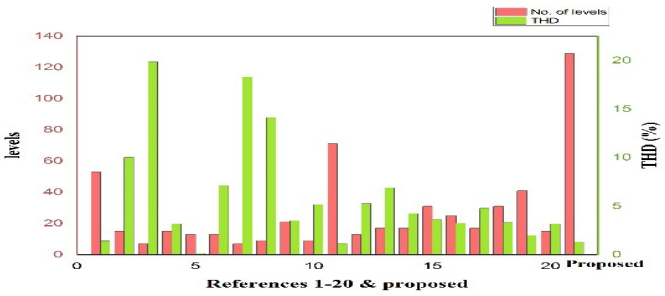

Fig. 26 No. of levels& Capacitors

V. CONCLUSION

A major advancement in power electronics has been made with the successful design and certification of a 129-level inverter that uses the Multicarrier Sine Pulse Width Modulation (PWM) control method, has fewer components, and has low Total Harmonic Distortion (THD). The suggested topology's dependability and efficacy are highlighted by the experimental and simulation findings' congruence. With its streamlined components, this inverter not only satisfies the need for cleaner power output in resistive and inductive load scenarios but also opens the door for improved efficiency and simplicity in multilevel inverter technology. The investigation continues even after we wrap up this project; rather, it is encouraged to continue in new directions. Alternative modulation methods, the inverter's performance under dynamic load scenarios, and application-specific design optimization are possible future research directions. The accomplishment of this 129-level inverter pushes the envelope of what is possible in the rapidly changing field of power electronics and paves the way for an exciting journey towards even more sophisticated and application-specific multilevel inverter designs.

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