Open & Short Circuit Fault Tolerant operation of 3 phase 2 level inverter for Permanent Magnet or Induction Motor Drive

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***Abstract*: The efficiency and reliability are the aspects of any electrical drive which attracts the customer towards it. Especially in case of EV the reliability is main issue. To make the EV more reliable the fault tolerant scheme of inverter for both permanent magnet and Induction motor drive have been explained here in this paper. The fault-tolerant operation (FTO) of the two-level inverter fed PM or induction motor for electric vehicle (EV) application. An introduction about open switch fault (OSF), short switch fault (SSF) and fault-tolerant operation of inverters is key aspects makes the drive more reliable. A simulation model for operation of the fault-tolerant is developed in MATLAB Simulink environment. The simulation model and results for fault-tolerant operation 2-level inverter fed induction motor & PM drive are shown.**

***Index Terms*—Open Switch Fault, Fault tolerant, detection, permanent magnet motor, voltage source inverter.**

I. I. INTRODUCTION

It is necessary to make the inverter system fault-tolerant because the device module accounts for about 34% of all defects [1]. Open switch fault (OSF) in power semiconductor switches used in the inverter is one of the primary causes of inverter failure [2]. As the number of switches increases, so does the likelihood of an open switch problem. Short switch faults (SSFs) are another kind of defect that can cause current to flow even when there is no gate pulse. Because of the increased current and junction warming caused by this failure, the switch blows [3]. As a result, the switch opens and later appears as having an open switch fault. The first type of cascaded H-bridge multi-level inverter (MLI) is a cascaded H-bridge three-level inverter. Switch-level, leg-level, module-level, or system-level fault-tolerant approaches can be used to make a cascaded H-bridge multi-level inverter fault-tolerant [4]. Since the structure of a cascaded H-bridge multi-level inverter is modular, module-level fault-tolerant techniques are typically used.The two main components of a fault-tolerant technique are fault-detection and fault-removal [5].

In order to identify the defective switch, a fault-detection method based on the error in phase-voltage across each HBridge, load current, and switching signal is presented in [6]. This fault-detection method was created after taking into account open switch faults caused by malfunctioning switching signals. It effectively identifies the issue with the H-bridge's two switches [7]. within one term of switching. This fault-detection technique's drawback is that it requires a specific amount of time (about five switching cycles or until the load current drops to zero) to identify the fault in two additional H-bridge switches [8]. This fault detection method has been documented for H-bridge inverter topologies with RL load or single-phase cascaded H-bridge three-level inverters. The only link voltage needed to operate each H-bridge is 40 V dc. The single-phase cascaded H-bridge five-level inverter (5LI) topology with RL load is another application of this fault detection approach in [9]. In [10], a fault-detection method for cascaded H-bridge multilevel inverters based on the half cycle mean voltage (HCMV) is described. This fault-detection method's drawback is that it requires around half a cycle of output voltage to identify an open switch fault [11], [12].

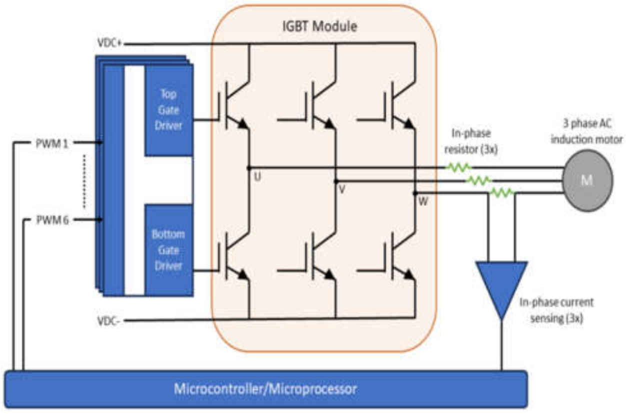

Fig. 1. Proposed topology for fault tolerant operation

The novel contribution of this paper are:

1. Fault-tolerant (FT) operation aims to detect the fault quickly in fraction of seconds
2. Reconfigure the drive continues running, usually in a degraded mode at reduced speed instead of total shutdown.
3. This is vital for safety-critical applications (EV, aerospace, industrial processes).

II. SYSTEM DESCRIPTION

A 3-phase 2-level voltage source inverter (VSI) is the most common topology used in motor drives (induction motors, PMSM), grid-tied systems, and renewable energy converters. It uses six power switches (IGBTs/MOSFETs with anti-parallel diodes) arranged in three legs (phases A, B, C). Each leg has an upper (high-side) and lower (low-side) switch connected across the DC bus shown in fig. (1).

Common Faults in Switches

1. **Open-circuit fault** (most studied): One (or more) switch fails to conduct (gate driver failure, bond-wire lift-off, etc.). Effect: Phase current loses half-wave highly

distorted currents, torque ripple, overheating, possible secondary faults. The inverter does not shut down immediately.

2. **Short-circuit fault** (more critical): Switch remains permanently ON (overvoltage, thermal failure, etc.).

Fault Detection Methods (Common for Both Open & Short)

1. **Current-based**: 3D current vector analysis, mean values of phase currents, current angle patterns, or residuals.
2. **Voltage-based**: Pole voltage residuals or switching state monitoring.
3. **Advanced**: Neural networks, observers, wavelet transforms, or machine learning for fast location (single/double faults).
4. Short-circuit often uses desaturation detection in gate drivers and fast fuses/hardware.

Fault Detection

The two steps of this fault detection technique are faulty phase leg identification and open and short switch fault detection. In [11], open switch fault isolation and detection are briefly discussed. Figure 2 shows a schematic design of the open switch fault detection technique for the S1a switch. Short switch failure detection hasn't been covered, though.

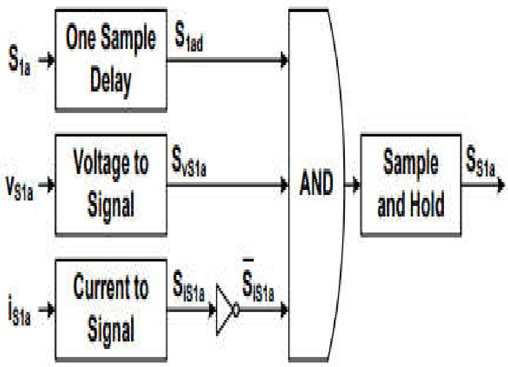

Fig. 2. Proposed fault detection logic

Figure 3. shows a schematic diagram of the suggested open and short switch fault detection scheme for the S1a switch. The sensed signals are sent through logic gates to produce the switching states of 0 and 1, respectively, under the switch's faulty and healthy conditions during open and short switch faults.

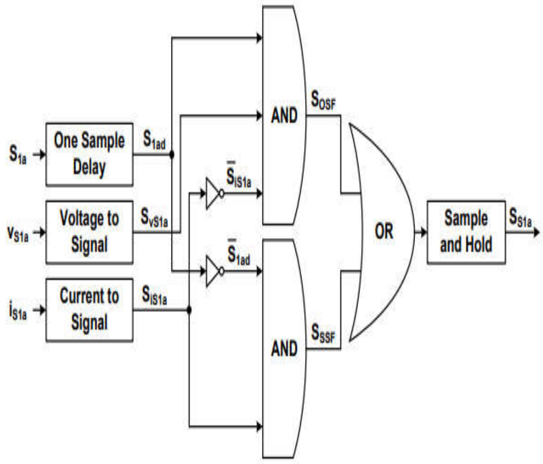

Fig. 3. Proposed OC and SC fault detection scheme

Table.1 shows the current state of the open switch fault (SOSF) detection logic. When the switch is in the ON state, the logic operation for an open switch fault is described as follows: "the switching signal" will be "high," and the sensed switch voltage (SvS1a) will be "high" (full value); in the faulty condition, the switch current (SiS1a) will be zero ("low") because the switch is open. Consequently, a NOT gate is used to invert the observed switch current signal.

TABLE I. LOGIC STATUS OF OPEN SWITCH FAULT DETECTION SCHEME.

Switch Condition	Sensed Signal			Signal Status			OSF Logic Status
	S1ad	vS1a	iS1a	SvS1a	SiS1a	(SiS1a)'	
Healthy	1	V_{sw}	Ia	0	1	0	0
	0	V_{dc}	0	1	0	1	0
Faulty	0	V_{dc}	0	1	0	1	1
	0	V_{dc}	0	1	0	1	0

Open switch fault logic is given by

$$Open\ switch\ fault\ logic = \mathrm{S1ad} * \mathrm{SvS1a} * (\mathrm{SiS1a})' \quad (1)$$

In the event of a malfunction, the combined result of the open and short switch fault detection system must be "high" (1), which will cause the bidirectional switching signal for the extra H bridge. The open and short switch fault detection output status Table 2 presents the logic. The switching signal's status is maintained by the sample and hold circuit. The remaining eleven switches (S2-4a, S1-4b, and S1-4c) have their switching signal statuses determined in a similar manner. An OR gate is added before the sample and held to obtain a high output of fault detection logic in either an open or short switch fault across any switch in order to have a comprehensive system for open and short switch fault detection

TABLE II. LOGIC STATUS OF SHORT CIRCUITSWITCH FAULT DETECTION SCHEME.

Switch Condition	Sensed Signal			Signal Status		SCF Logic Status
	S1ad	vS1a	iS1a	S1ad′	SiS1a	
Healthy	1	V_{SW}	Ia	0	1	0
	0	V_{dc}	0	1	0	0
Faulty	1	V_{SW}	Ia	0	1	0
	0	V_{SW}	Ia	1	1	1z

$$Short\ circuit\ switch\ fault\ logic = (\mathrm{S1ad})' * \mathrm{SiS1a} \quad (1)$$

Open switch fault (OSF):

During the open switch fault, the current through the switch is zero and the voltage across the switch is V_{dc}, if lower switch in same leg is conducting and $V_{dc}/2$, when the the lower switch in same leg is not conducting. During the open switch fault (OSF), motor speed decreases to maintain the constant torque and the torque ripple increases because two phases carry the load current, which would otherwise be in three phases. To maintain equilibrium, there is an increase in current of the healthy phases. The stator currents during the six distinct states over a complete cycle are given in Table II.

In Table II, V_{dc} is the DC link voltage, E_{ab}, E_{bc}, E_{ca} are line back emfs, and I_a, I_b, I_c are stator currents of the BLDC motor. The equations obtained in Table II represent the stator currents obtained in six distinct sectors. These are found by applying Kirchhoff's voltage law in the six different sector . The surge in the healthy phase current creates a problem to remaining healthy switches. So preventive fault tolerant operation is required. From Table II it is observed that during OSF in switch S_1, in sector 1 and sector 2 there is no current in any of the phases, so motor gets retarded in this period and then again in sector 3 to sector 6 motor tries to regain its original speed, this causes high ripple in torque and current drawn from healthy switches. This unbalancing of current produces high ripple in torque and creates drive operation unstable. So to protect the remaining healthy switches, the faulty switch has to be replaced by healthy switch.

Short switch fault (SSF):

The SSF is mainly due to current overloading or melting of bounding wires, short circuiting drain to source. During short circuit the voltage across the switch becomes very low almost zero and current through the switch is always there. In one third period of an electrical cycle, it shorts the battery or DC link, hence a very high current flows which harms the battery or DC link capacitor. So the SSF have to be detected and removed.

III. FAULT TOLERANT OPERATION

Fault tolerant operation during OSF classified into two section, first isolation of faulty leg and second replacing the faulty leg with healthy auxiliary leg.

Isolation of faulty leg:

After detection of OSF, the complete phase or leg have to be replaced by a healthy leg. For this the second switch of the faulty switch leg have to be turned off. Then the complete leg is replaced. The removal of faulty leg has been explained through the following

Let the OSF occur at switch 1, then there is no impact of gate signals, the current through the switch is zero. The realization of fault has been performed within two sample time. From Table III, the high signal indicates the fault. The same signal is hold and used to isolate switch 2, as well as for connecting the healthy auxiliary leg in place of faulty switch leg. The mode 1 operation logic is explained with the help of Fig. 3.

Replacing faulty leg with auxiliary healthy leg:

If Sau is high, it indicates the fault in switch 1, then it is used to isolate phase ‘a’ leg, and replace it with auxiliary phase a leg as explained through logical circuit of Fig. 4.

Replacing faulty leg with auxiliary healthy leg:

If Sau is high, indicates the fault in switch 1, then it is used to isolate phase ‘a’ leg, and replace it with auxiliary phase a leg as explained through logical circuit of Fig. 4.

Here Sauh is the hold high signal, S_{G2m} is modified gate signal used for switching the switch S_2, $S_{Ga1}$and S_{Ga2} are the auxiliary healthy leg signals.

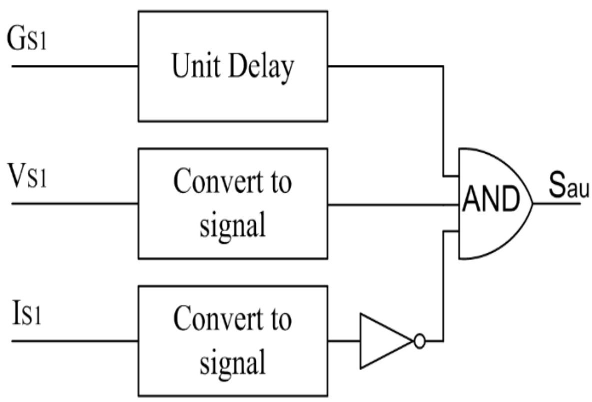

Fig. 4. Logical circuit for fault detection

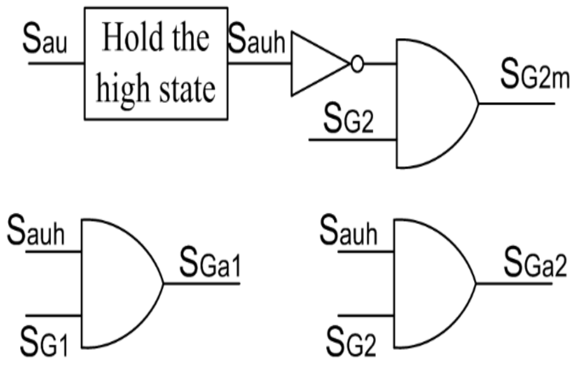

Fig. 5. Logical cicuit for fault- tolerant operation

IV. Circuit Description

The fault tolerant two level VSI is presented in this section. The schematic diagram for two level inverter with fault tolerant operation is shown in Fig. 5, on the left side of BLDC motor the switches are main converter switches and on the right side the switches are auxiliary converter switches. The proposed circuit consists of 12 IGBT as switches i.e. six main operating switches and six auxiliary switches, one auxiliary switch for each main switch. In the proposed research, during fault tolerant operation the complete leg is isolated if any of the switch of a particular leg suffers from OSF. This fault tolerant operation also requires six voltage and six current sensors to sense the voltage across and current through all the switches. The sensed voltage and current are transferred to the logic shown in Table III in the signal form. Fig.5. shows the healthy or normal operation of inverter, where six main switches are working.

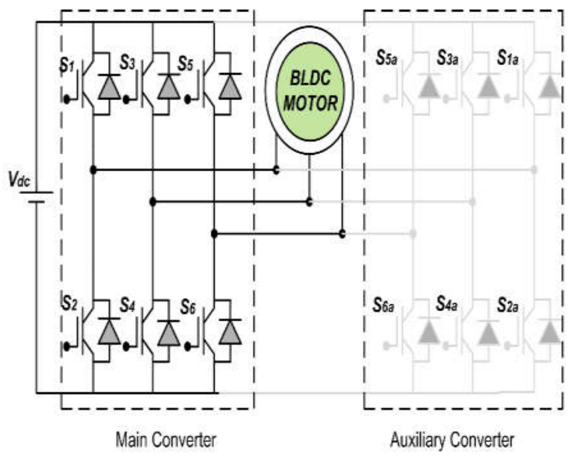

Fig. 6. Schematic for Fault tolerant operation

Fig. 6 shows the condition when either or both switch of leg 1suffer from OSF. So faulty leg is replaced by auxiliary backup leg of VSI. Similarly in Fig. 7 and Fig. 8, switches of phase b and phase c suffer from OSF respectively and fault tolerant operation carried out by replacing the faulty leg with healthy leg through respective auxiliary backup legs of inverter. Fig. 9 shows the block diagram representation of the experimental setup for the proposed configuration. The control section consists of Host PC, micro lab box 1201(real time controller), and voltage sensors (LV 25P) as well as current sensors (LA 25P). Host PC perform all the logicalfunctions, which is actuated by the DSP based processor.The outputs are taken through digital input output (DIO) pins.The sensors connect the power circuit to control circuit.The power circuit consists of 3-φ AC mains supply, 3-φ Auto transformer, two voltage source inverter (VSI), and BLDC

V. Results and Discussion

The results of fault tolerant operation are obtained by recording the waveforms of gate switching signals for upper switch of phase a, phase b, and phase c. OSF is created in upper switch of leg a, thereafter auxiliary backup leg gets switching signal. The MATLAB simulation results are observed

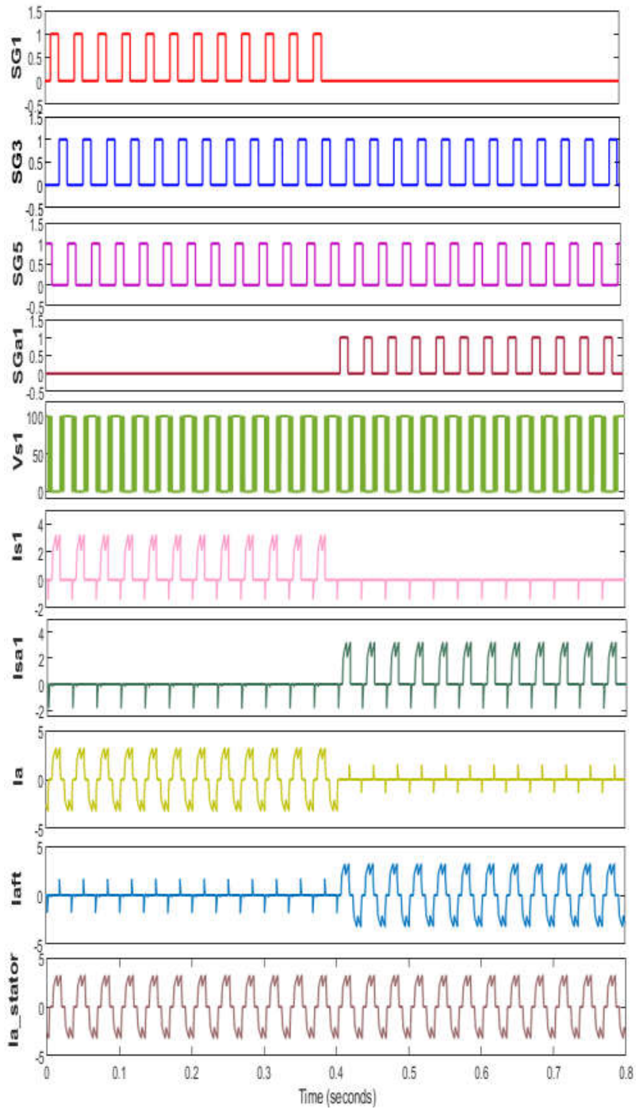

Fig. 7. Two level Inverter with fault tolerant capability suffers from OSF in Sw 5 or Sw 6.

VI. Conclusions

This paper presented a simple logic-based fault tolerant operation for open switch fault in voltage source inverter. The proposed scheme successfully implemented in MATLAB Simulink platform successfully identified the faults and then able to replace the faulty leg with healthy leg quickly and effectively, without interrupting the motor operation. This work is based on the simple logical operation, so speed is not a constraint. Experimental results verify the logic successfully, then fault tolerant operation for SSF shall be obtained in future.

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