Design & Implementation of an efficient 1-bit Hybrid Full Adder

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***Abstract*— The demand for low-power and energy-efficient computing devices is rising rapidly. An adder stands as a fundamental component in these devices. Hence, its power consumption needs to be minimized. A 1-bit hybrid full adder employing transmission gates and complementary metal oxide semiconductor logic is presented in this paper. It provides full swing outputs and consumes very low power in comparison with other presented designs. The layout design, simulation and performance measurement are done in 45 nm technology.Efficient power management is essential for achieving high-speed performance in electronic devices. Furthermore, the area overhead of the proposed design is also less when compared to existing designs.**

***Keywords*—**Hybrid style adder, transmission gates.

I. INTRODUCTION

The reliance on mobile electronic gadgets and computing tools such as cellular phones, smart watches, and palmtops is increasing, making them integral to our daily lives. Design engineers are striving to develop low-power, high-speed, and energy-efficient circuits to optimize the performance of these devices. However, designing a low-power consuming circuit is challenging due to the increasing system clock frequency and involvement of different system abstraction levels [1].

A full adder is a fundamental component in almost every arithmetic circuit, including subtractors, multipliers, and dividers, and it is often part of the critical path in many circuits [2]. Enhancing the performance of the full adder at the basic stage can effectively improve the overall system performance. A logic circuit is classified as a full adder if it produces outputs, Sum and Cout, for the inputs A, B, and Cin [4], where:

$$Sum = A \oplus B \oplus Cin. \quad \text{.....(1)}$$

$$Cout = A \cdot B + B \cdot Cin + A \cdot Cin \ldots \quad (2)$$

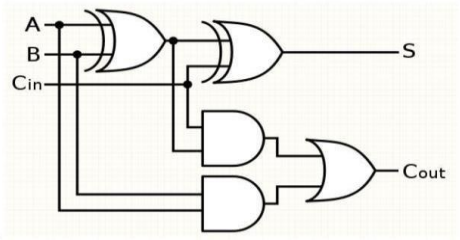

FIG 1: Full Adder using XOR gates

Several performance parameters, such as total power, propagation delay, and power-delay product (PDP), are associated with a full adder circuit. Optimizing the size of the transistors is an effective approach to reduce the total power consumption of the circuit. Furthermore, the aforementioned parameters can be further improved by employing different transistor arrangements in the layout [6].

To minimize power consumption, wiring complexity, area, and delay of a full adder circuit, various logic styles can be utilized [7]. Each logic style possesses unique characteristics, which may differ from one

TABLE 1: Truth Table of full adder

A	B	Cin	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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II. LITRATURE SURVEY

A. M. Shams and M. A. Bayoumi, [1] A novel 16-transistor CMOS 1-bit full-adder cell is introduced, incorporating low-power designs of XOR and XNOR gates, pass transistors, and transmission gates. This cell delivers enhanced speed and reduced power consumption compared to conventional 1-bit full-adder implementations. Its high speed is attributed to the elimination of an inverter from the critical path, while the reduction in the number and magnitude of cell capacitances, along with the elimination of the short circuit power component, contributes to its low power consumption.

S. Akhter, S. Chaturvedi, S. Khan and A. Bhardwaj, [2]This paper presents a novel topology for a dynamic logic-based full adder, which utilizes modified architectures of XOR and XNOR logic gates as basic building blocks. The suggested topology of XOR/XNOR gates provides a full logic swing, which is advantageous for the implementation of the full adder circuit. The proposed full adder circuit is simulated using conventional 180 nm CMOS process technology, and the results obtained through SPICE simulation tool demonstrate significant improvements in power dissipation and speed compared to earlier reported designs.

P. Agrawal, D. K. Raghuvanshi and M. K. Gupta,[3]. The paper introduces a novel model of a low-power 1-bit hybrid adder that combines CMOS and Transmission gate technologies to produce full swing outputs. The proposed adder is compared with existing designs, including Conventional-CMOS (C-CMOS), CPL, TGA, 14T, 24T hybrid adder, and 16T hybrid adder, in terms of power, delay, and power-delay product in 180-nm and 65-nm technology.

The simulations were conducted using the Spectre simulator on Cadence Virtuoso for various voltages and frequencies. The results indicate that the proposed adder consumes 35-40% less power than C-CMOS and is 25-50% faster than C-CMOS.

A. M. Shams, T. K. Darwish and M. A. Bayoumi [4].The paper presents a comprehensive performance analysis of a 1-bit full-adder cell. The full-adder cell is divided into smaller modules, which are thoroughly studied and evaluated. Multiple designs of each module are developed, prototyped, simulated, and analyzed.
Using different combinations of these module designs, twenty distinct 1-bit full-adder cells are constructed, with most of them being novel circuits. Each of these cells demonstrates varying power consumption, speed, area, and driving capability figures.

M. Suzuki et al, [10].The paper describes a 32-b CMOS ALU (arithmetic and logic unit) that is fabricated using 0.25-μm CMOS technology and has a 1.5-ns addition time with a 2.5-V supply. This fast addition time is achieved by utilizing double pass-transistor logic (DPL) and a conditional carry-selection (CCS) carry look-ahead circuit. The paper also presents the measured supply-voltage dependence of ALU addition time, which demonstrates excellent low-voltage performance. Additionally, the paper reports that DPL AND/NAND and OR/NOR ring oscillators exhibit measured speed improvements of 15% and 30%, respectively, over CMOS NAND and NOR ring oscillators.

III. PROPOSED METHODOLOGY

Dividing a full adder into different modules enables the separate analysis, optimization and testing of each module.

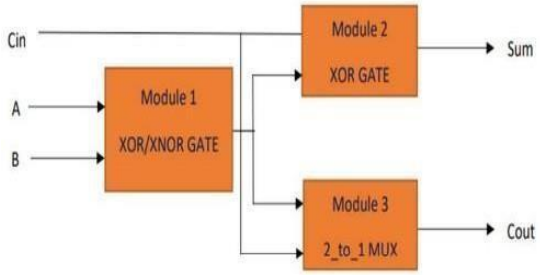

FIG2: Modules in a full adder cell.

Module-1: The XOR and XNOR gate circuits in this module exhibit excellent driving capability. In the proposed design, the XOR circuit generates a full swing output, while the XNOR circuit produces a satisfactory voltage swing.

Module-2: The delay of the SUM signal is also optimized here. The conditions for SUM output generation is as follows:

If, Cin = 0, SUM = XOR;

Else, SUM = XNOR

The logical condition used for level restoring transistors is as follows

If, A = B, SUM = Cin.

Module-3: Carry output (Cout) is generated in this module using two transmission gates. The utilization of transmission gates ensures the further reduction in propagation delay. These gates use the following conditions to generate carry output:

If, A = B, Cout = B; else, Cout = Cin.

IV. REQUIREMENTS

Cadence Virtuoso

V. IMPLEMENTATIONS

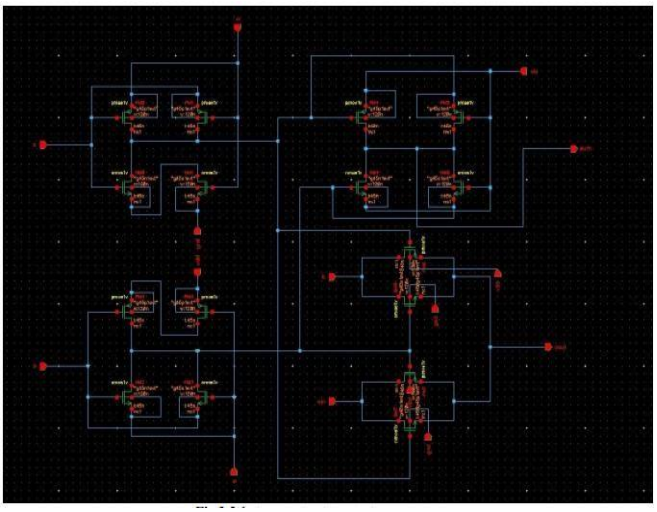

FIG 3: Schematic of hybrid full adder.

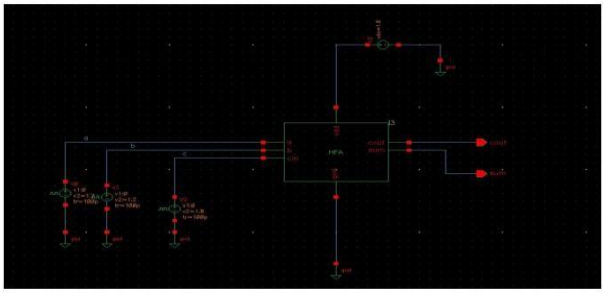

FIG 4: Testbench of hybrid full adder

The provided figure 3 illustrates the proposed hybrid full adder. The XOR gate is implemented using transistors P1, N1, P2, and N2, while the XNOR gate is implemented using transistors P3, N3, P4, and N4. These gates generate output signals based on the logic conditions of the inputs, A and B. These signals are then utilized in Module-II, with logic conditions of Cin, to generate a full swing SUM signal. In this module, transistors P6 and N6 are controlled by the input Cin to provide the SUM signal, and the voltage degradation in the output is eliminated using two-level recovering transistors, P5 and N5. In Module-III, XOR and XNOR signals are employed for switching. The full swing carry output is generated using two transmission gates, realized using P7, N7, P8, and N8.

When inputs A and B are equivalent, the Cout is identical to input B; otherwise, the input Cin is replicated as Cout. Additionally, the sizing of this module ensures low power and delay.

TABLE I

Transistor Sizes Of The Proposed Hybrid Full Adder Cell

Transistor	180 nm Process		90 nm Process	
	Width(nm)	Length(nm)	Width(nm)	Length(nm)
N1	400	180	120	90
P1	800	180	360	90
N2	800	180	240	90
P2	1200	180	420	90
N3	400	180	120	90
P3	800	180	360	90
N4	400	180	180	90
P4	1600	180	540	90
N5	400	180	160	90
P5	400	180	400	90
N6	400	180	160	90
P6	400	180	400	90
N7	400	180	360	90
P7	800	180	540	90
N8	400	180	360	90
P8	800	180	540	90

VI. RESULTS

TABLE 3. COMPARISION TABLE.

Full Adder Circuit	Power (uW)	Area	Delay (ps)
Hybrid_FA[12]	36.46	22	32.28
Valashani_FA[14]	18.36	18	33.15
Proposed	5.171	16	29.16

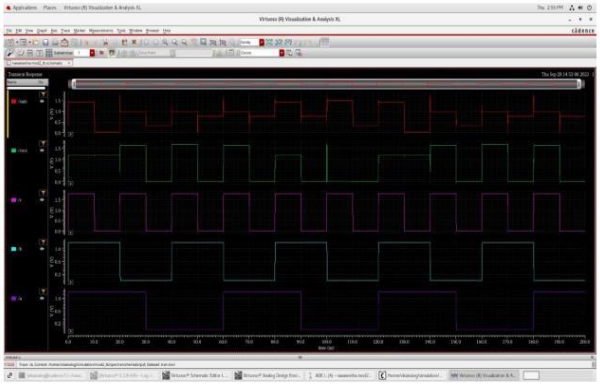

FIG: 5 Input –output waveform of hybrid full adder

The proposed 1-bit hybrid full adder cell is implemented on a 45nm process node, with a voltage of 1.2V. Inputs A, B, and Cin are used with different periods for simulation, while SUM and Cout are the outputs. The input and output waveforms of the proposed hybrid full adder design are depicted in Fig. 5. Inputs A, B, and Cin, with time periods of 80ns, 40ns, and 20ns, respectively, are applied to the proposed full adder as inputs, and the outputs are observed as SUM and Cout signals. The outputs are found to be full swing with minor glitches, as shown in Fig. 5. The performance evaluation of the proposed full adder circuit, based on total power and propagation delay, in comparison to other available circuit designs, is presented in Table 3. The unit of power is taken as microWatts (µW), and the delay is measured in pico-seconds (ps).

VII. CONCLUSION AND FUTURE SCOPE

The project introduces a low-power, 16-transistor full adder based on hybrid logic style. The simulation results demonstrate that the presented full adder delivers full swing output with enhanced performance across all considered parameters. The proposed full adder circuit exhibits improvements in total power, delay, and a slight reduction in layout area compared to previously proposed hybrid full adder circuits. Furthermore, the proposed hybrid full adder cell can be expanded for higher bit orders for multiple-bit operations, and its design can be further enhanced using different transistor arrangements to achieve improved performance parameters. Additionally, it holds potential for various applications such as low-power computing devices, multipliers, and ALUs.

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