Time and Frequency Domain Approach for Examining Stability of DC-DC Boost Converter

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Abstract.

This study gives the frequency and time domain approach with balance evaluation of a boost dc-dc converter through acquiring the zeros and poles values. Kirchhoff's Current and Kirchhoff's Voltage regulations (Laws) can be used to determine the dynamic behaviour of DC-DC boost circuit. To look into the structuring found in each ideal and non-ideal circuits, we will use MATLAB software, that is a programming platform for comparing and building machine platforms, growing increase converter circuits, and visualising output waveforms. It evaluates the systems stability balance using the most adopted techniques like root locus technique, Nyquist stability criteria, and bode plot methodologies, as well as providing additional information on the system's characteristic and pole placement.

Keywords. Boost dc-dc converter, Poles and Zeroes, Laplace transformations, Root locus technique, Nyquist stability criteria, Bode plot.

1. INTRODUCTION

A boost converter is a DC-DC converter that produces greater output voltage as compared to the input voltage. It's also known as a step-up converter since it boosts the output voltage. Because of the need to keep power running to conserve energy, the supply current is bigger than the output current. When a system deviates from its equilibrium state, noise and disturbance increase, and the output becomes unbounded. A powerful system, on the other hand, sticks to the Bounded-Input Bounded-output (BIBO) situation and returns to its equilibrium point. The state diagram version can be used to investigate the zeros and poles of the converter [1]. The frequency of zeros is calculated, allowing for a better understanding of the reason for zeroes in boost converters. Although signal flow with the graphs are used to compute the switch characteristic, they seldom provide data at the beginning of the poles and zeros detected inside the resulting [8] transfer function.

On this research, the balance of a boost DC-DC converter is evaluated, which is utilised to increase the amplitude of a specified input voltage to a very excessive level. The typical boost DC-DC converter is shown, which includes an inductor for energy storage before being sent straight to the load, guaranteeing that the amplitude signal is raised, also known as amplification. We will gather the switch characteristic or circuit equations utilising this increase converter, as well as Kirchhoff's voltage and modern laws in common usage. This examination aids s-domain evaluation over time-domain evaluation for the boost converter, which is an electrical circuit with variable voltage and modern alerts and may be thought of as a simple resistive network. The steadiness of a boost converter, which is utilized to build plentifulness of information related to a given voltage to an extremely undeniable level, is inspected in this test.

The first boost DC-DC converter is shown, which incorporates an inductor for energy storage before being supplied directly to the load, resulting in amplification (sign amplitude rise). We may obtain the switch characteristic or circuit equations using this boost converter and Kirchhoff's voltage and contemporary legal guidelines in a common approach. This examination favours s-domain evaluation over time-domain evaluation since the boost converter is an electrical circuit with variable voltage and modern alerts and may be thought of as a simple passive circuit consisting of resistive elements. The employment of loop rules in s-domain circuit prevents differentiation and integration at the same time. The resultant network is then characterised as a closed loop control system with a feedforward network along with an advantage to have a feedback gain. The switching characteristics of the system are obtained after obtaining the closed-loop system, and the stability is determined using the most widely used root locus technique [9-11], Porter stability method [12][13] and Nyquist stability criterion Equilibrium [14] calculation]. All mentioned methods are acceptable since they allow the definition and estimation of relative stability [15]. Use MATLAB to evaluate stability testing of boost converters to verify theoretical, computational, and practical results.

2. MODELLING OF EQUATIONS

The primary potential of an inductor to resist modifications via way of means of boosting or reducing the electricity saved with inside the inductor magnetic subject is the important thing aspect that powers the boost converter.

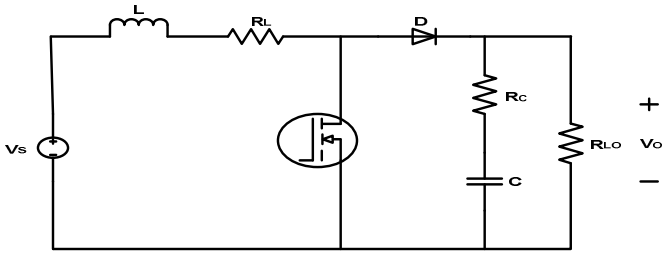

Fig. 1. Boost Converter

Figure 3 shows the boost converter circuit having input Vs, N-MOSFET as switching device, duty cycle input k, diode D and inductor L with lumped additive, capacitor C and load resistor R_{LO}. To prevent the effects of excessive current, resistors RL and RC are coupled with the inductor and capacitor. Then check the following circuit.

2.1. When Switch is ON: 0 < t < (t = kT)

In Figure 4, the converter circuit is illustrated running at a time interval of (0 < t < (*TON* =kT)). The N-MOSFET operates as closed switch as a voltage-controlled device ($Vs>V_{threshold}$). The diode is opposite one-sided and open circuited because of the negative charge at the anode.

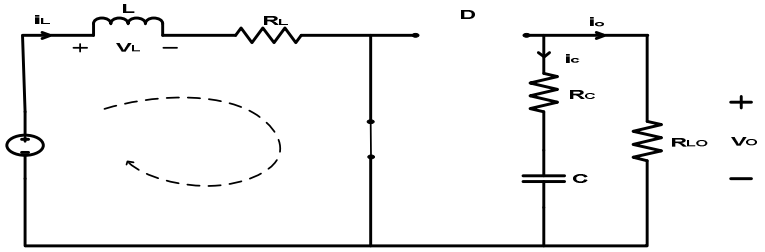

Fig. 2. When Switch is ON

At this moment, the inductor is charged to VL. With connection with the 0 preliminary conditions, the switching ON circumstance time is then derived as:

$$V_s = V_L \quad (1)$$

$$V_s = L_{i_L} + i_L R_L \quad (2)$$

On applying Laplace transformation to equation-2

$$V_S = Ls_{i_L(s)+i_L}(s)R_L \quad (3)$$

$$i_L(s) = \left(\frac{V_S}{L}\right) \cdot \frac{1}{S+\frac{R_L}{L}} \quad (4)$$

On applying inverse Laplace transformation on equation (4)

$$L^{-1}[i_L(s)] = \frac{V_s}{L} L^{-1}\left[\frac{1}{S+\frac{R_L}{L}}\right]$$

$$\int_{\mathrm{Im}\,in}^{\mathrm{Im}\,ax} i_L(s)\,dt = \frac{V_s}{L}\int_0^{T_{ON}} \frac{1}{S+\frac{R_L}{L}}\,dt$$

$$[\mathrm{Im}\,ax - \mathrm{Im}\,in] = \frac{V_s}{L}\cdot e^{\frac{-R_L}{L}t} \tag{5}$$

$$\Delta I_L(ON) = \frac{V_s}{L}e^{-\frac{R_L}{L}kT} \tag{6}$$

2.2. When Switch is OFF: (T_{ON}=kT) < t < T

Figure five shows the circuit for the condition ((TON=kT) < t < T). As of now, the inductor has been charged to Vs - Vo - iL(t)RL, the diode is shut when the switch is opened.

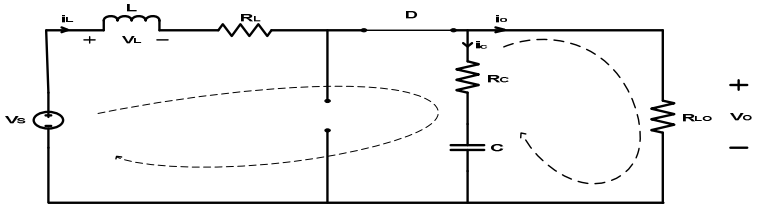

Fig. 3. When Switch is OFF

The time it takes to turn off is computed as, assuming that the beginning situations are zero.

Applying KVL, we get:

$$V_s + V_L - V_0 = 0$$

$$V_L = -[V_s - V_0] \tag{7}$$

Applying KCL at node 1: we get,

$$i_L = i_c + I_0$$

$$i_C = i_L - I_0 \tag{8}$$

Average output voltage Vo can be evaluated by:
During T_{OFF} => S = OFF and D=ON
The inductor is charged upto:

$$V_s - V_0 - V_L = L\frac{di_L}{dt}$$

$$V_s - V_0 - i_L(t)R_L = L\frac{di_L}{dt} \tag{9}$$

By applying Laplace transformation on equation (9), we get:

$$V_s - V_0 - I_L(s)R_L = LsI_L(s)$$

$$I_L(S) = \frac{\frac{V_s - V_0}{L}}{s+\frac{R_L}{L}} \tag{10}$$

By performing the inverse laplace transformation on (10),

$$L^{-1}[I_L(S)] = \frac{V_s - V_0}{L}\cdot L^{-1}\left[\frac{1}{s+\frac{R_L}{L}}\right]$$

$$I_L(t) = \frac{V_s - V_0}{L}\cdot e^{-\frac{R_L}{L}(t)} \tag{11}$$

For t = (1-K)T and $I_L(t) = \Delta I_L(0FF)$

Hence,

$$\Delta I_L(OFF) = \frac{V_S - V_0}{L} \cdot e^{-\frac{R_L}{L}(1-K)T} \quad (12)$$

By setting the total of the ON and OFF currents to zero, we can calculate the output voltage as a function of the inputting voltage (V_s), series resistance (R_L), and duty cycle component (k) of the N-MOSFET,

$\rightarrow \Delta I_L(0N) + \Delta I_L(OFF) = 0$

$$\frac{V_S}{L} \cdot e^{-\frac{R_L}{L}(KT)} + \left(\frac{V_S - V_0}{L}\right) \cdot e^{-\frac{R_L}{L}(1-K)T} = 0$$

$$\frac{V_0}{V_S} = e^{-\frac{R_L}{L}(2KT-1)} + 1 \quad (13)$$

Eqn. (13) is used to compute the output to input voltage ratio in time domain, the duty cycle appears to be the key determinant of the ratio. You get a transfer function when you apply the Laplace transform to the ratio of two values (13). We may change the switching ON and OFF periods and analyse the stability independently for each scenario by modifying the duty cycle (k), as illustrated in Figs. 4 and 5.

Using numerous ahead paths from input to output, [1] investigates the origins of zeros and their placement.

3. RESULTS AND DISCUSSION

3.1. Ideal and Non-Ideal cases of DC-DC Boost Converter

The circuit evaluation including simulation results discovers are isolated into classifications relying upon the ideal or non-ideal of lumped parts like inductors and capacitors. This section will go into the proposed work's modelling and design. The prescribed work shows how to operate and control a boost converter with a scope of elements that are well defined for various circumstances.

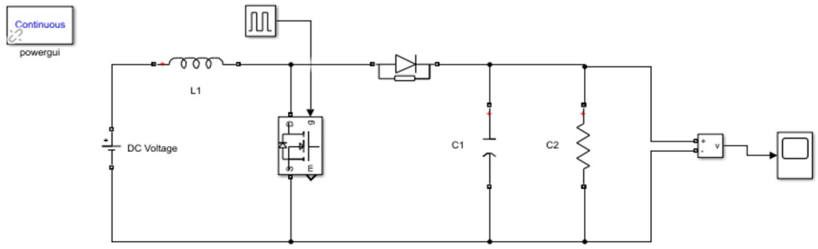

Fig. 4. Simulink model of DC-DC Boost converter (Ideal case)

Figure 4 shows the circuit diagram of a boost-DC converter without considering the internal resistance of the inductor and capacitor, that is the ideal situation.

SERIAL NUMBER	PARAMETER	RATING
1	DC Input Supply (V_{DC} /V_{INPUT})	5V
2	Pulse Generator Amplitude	1
3	Pulse Generator Period (s)	1/25000
4	Pulse Generator Phase Delay	0
5	Diode R_{ON}	0.001 ohm
6	Diode V_f(Forward Voltage)	0.8V
7	Inductance	1mH
8	Capacitance	33 µ F
9	Load Resistance (R_{LOAD})	100 ohm

TABLE I. Specifications For K=25% (assuming Ideal Case)

The above-mentioned simulation parameters are for output voltage for duty cycle ratio k=25%(IDEAL CASE)

The value of the output voltage rises dramatically, indicating that the output voltage has been raised. Based on duty cycle, the obtained result through simulation of the model shown in Fig.6 is further categorised into two further modes (k=0.25 – in Fig.5 and k=0.50 – in Fig.6).

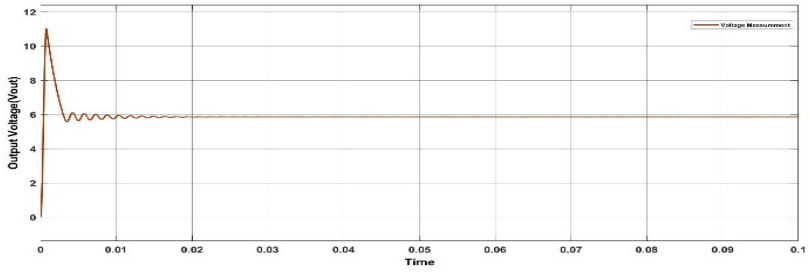

Fig. 5. Output response for 25% of duty cycle

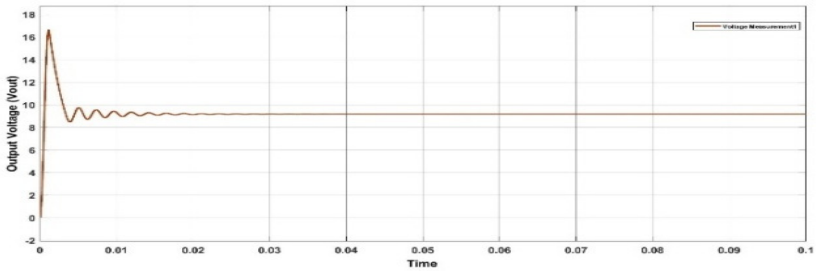

Fig. 6. Output response for 50% of duty cycle

In the cases presented below, the passive components inductors and capacitors are assumed to be non-ideal, and the circuit is evaluated for a number of non-ideal cases.

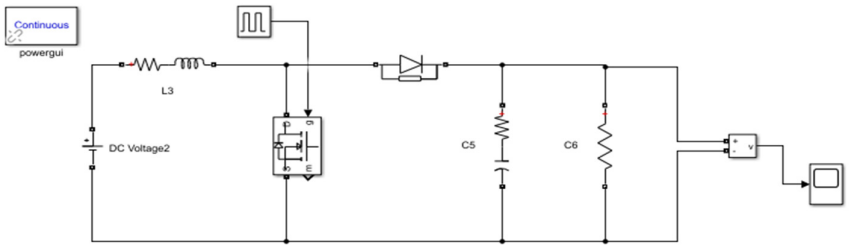

Fig. 7. Simulink model of DC-DC circuit (Non-ideal case)

The simulated outcome is separated into two further modes based on various duty cycle values, as shown in Fig.7 (k=0.25 – in Fig.8 and k=0.50 – in Fig.9).

SERIAL NUMBER	PARAMETER	RATING
1	DC Input Supply (V_{DC}/V_{INPUT})	5V
2	Pulse Generator Amplitude	1
3	Pulse Generator Period (s)	1/25000
4	Pulse Generator Phase Delay	0
5	Diode R_{ON}	0.001 ohm
6	Diode V_f(Forward Voltage)	0.8V
7	Inductance	1mH
8	R_L	5Ω
9	Capacitance	33 µF
10	R_C	5Ω
11	Load Resistance (R_{LOAD})	100 Ω

Table II. Specifications for k=25% (non-ideal case)

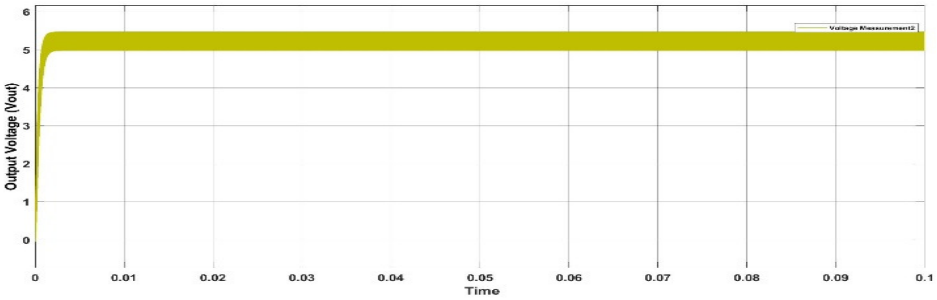

Fig. 8. Output response (including RL and RC) for 25% of duty cycle

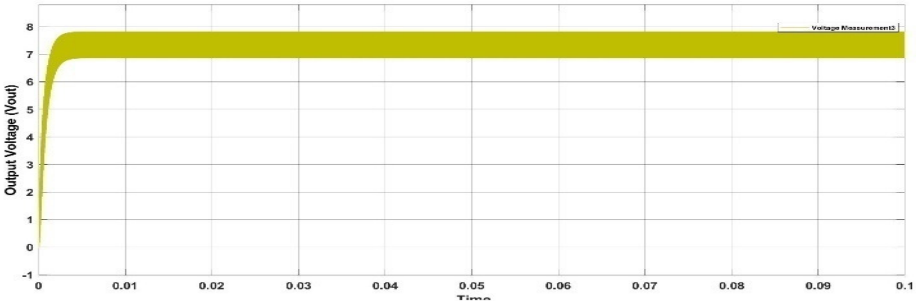

Fig. 9. Output response (including RL and RC) for 50% of duty cycle

In this case, comparable outputs or outcomes are obtained, i.e., the output voltage will increase greatly while in comparison to the input voltage; however, the graphs in the preceding instances are in a very one of a different sequence. The first graph looks as if a second-order system's output plot, while the second one graph looks as if a first-order system's output plot. The same two instances are depicted in this brief, but the capacitance value has been modified.

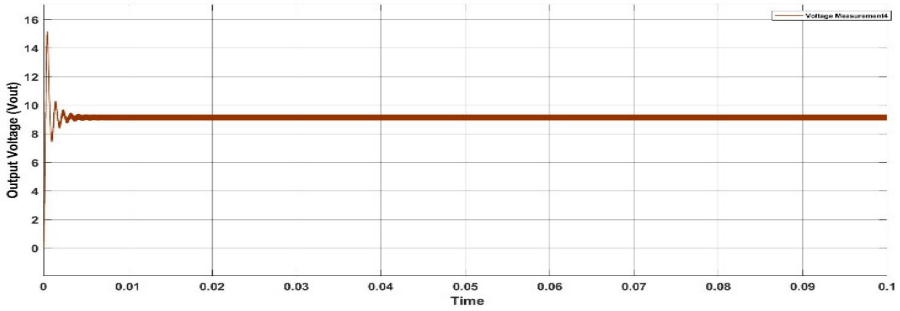

Fig. 10. Output response (assuming ideal case) for C = 5 µF

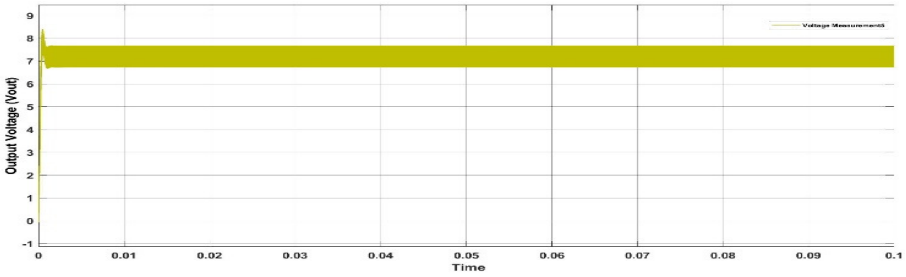

Fig. 11. Output response (assuming non-ideal case) for C = 5 µF

Figure thirteen depicts a non-ideal boost converter with a five MICROFARAD capacitance and a 0.5 duty cycle.The time scale is downscaled as the capacitance is decreased, expanding the frequency of the response, as displayed in the graphs above.

3.2. Stability Analysis

The stability analysis gives a deep insight into the working model of chosen Boost-converter circuit. The stability analysis has been implemented using time domain approach with reference to root locus and frequency domain with reference to bode plot and Nyquist stability criteria. The analysis has been carried out in terms of varying duty cycles viz., for 5%, 10%, 25% and 50%..

3.2.1 Root Locus Technique

Root locus technique is a graphical approach used in control theory and stability examinations to effectively analyze the systems behaviour based on change or updation of a parameter like the gain in a feedback system and/or effectively analyze the change in systems behaviour on adding a pole or a zero to the existing system.

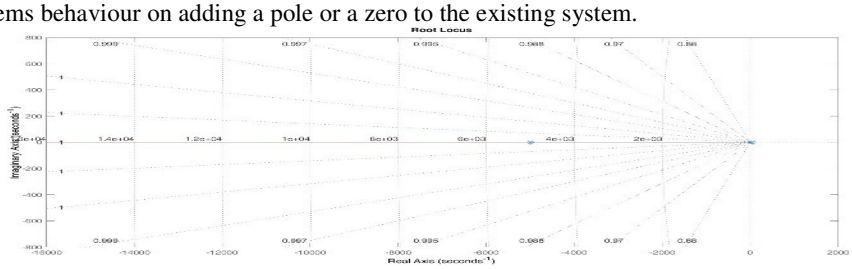

Fig. 12. Root Locus plot for k = 0.25

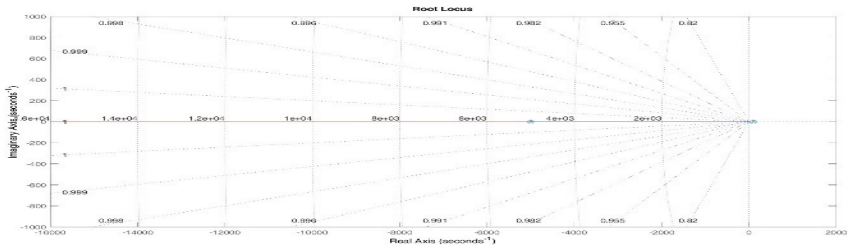

Fig. 13. Root Locus plot for k = 0.50

The position of the pole is affected by the gain of the system. Therefore, root locus trajectories help to graphically locate all possible positions of the system's characteristic roots (poles) on the S-plane. So by analyzing the transfer function, we found that the system is stable when the duty cycle is 1%, 5%, 25%, and 50%.

3.2.2 Nyquist Plot

A Nyquist plot is a parametric frequency response map used in automated control and signal processing. Nyquist plots are most commonly used to test the stability of a feedback system.

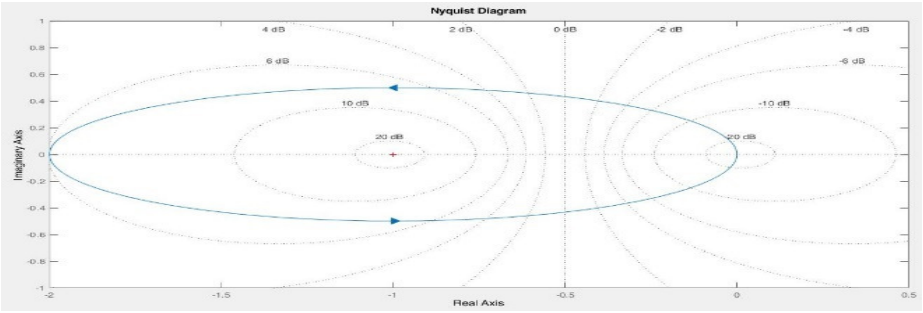

Fig. 14. Nyquist plot for k = 0.50

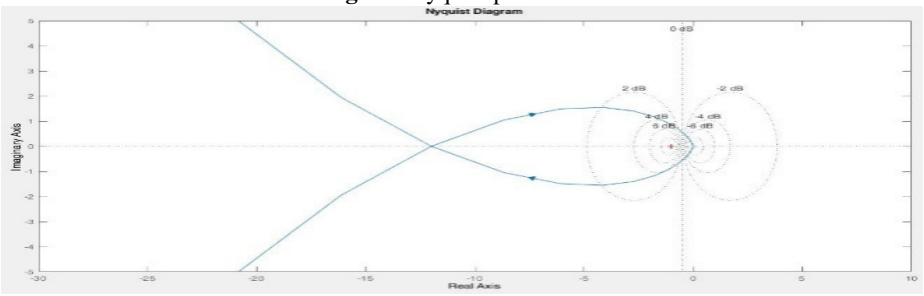

Fig. 15. Nyquist plot for k = 0.60

To assess the control system to be completely stable, marginally stable or completely unstable, the plots based on Nyquist criteria are examined. The metrics gain as well as phase margin are examined in particular. In our Nyquist plot, we get a unit circle. For stability criteria, if the unit circle direction is in anti-clockwise, then it is said that the system is stable and if the unit circle is in clockwise direction, the system is said to be unstable. As same for root locus plot, for 50% duty cycle it is stable but for 60% duty cycle it is unstable.

3.2.3 Bode Plot Technique

A Bode plot evaluation is used to expose the benefit and segment reaction of our system at numerous frequencies. A part of graph representing the log-amplitudes (measured in dB, a unit to represent on a logarithmic scale) of the transfer function and frequency is displayed in the figures below. Because of its logarithmic scale, the Bode plot is ideal for displaying functions with several orders of magnitude of variance.

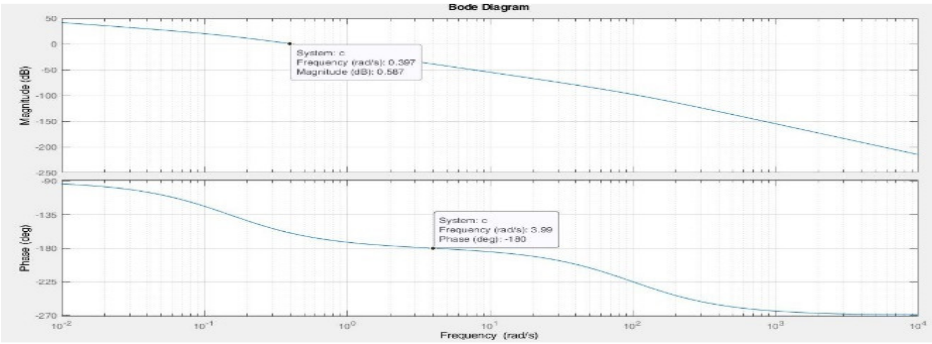

Fig. 16. Bode plot for k = 0.50

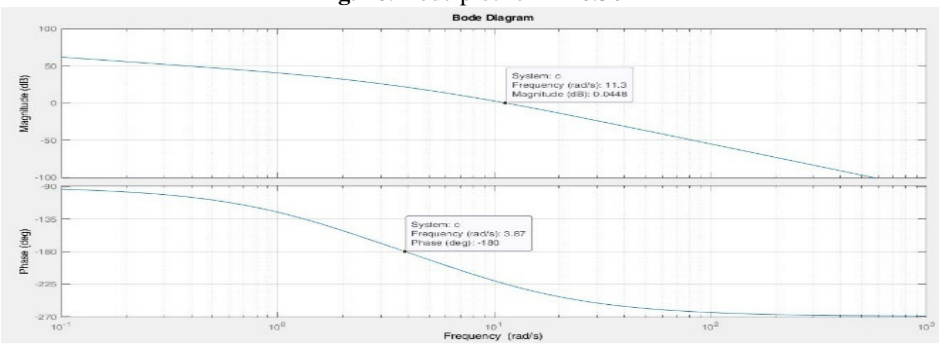

Fig. 17. Bode plot for k = 0.60

Here for the duty cycle k equal to 5%, 10%, 25% and 50% the system is stable but when duty cycle increases i.e., for k equal to 60% it is said to be unstable. It is also obvious from the transfer function that it has just one pole at the origin. The benefit of this technique is that it offers insight into how the circuit elements impact the system's frequency response, which is more predominant in the structural design of boost converter circuits.

4. CONCLUSION

Based on the basic design of a DC-DC boost converter, its equivalent mathematical model is considered for developing the model representing the transfer function in terms of laplace transformations. The mathematical equivalence as a transfer function, gives a simple and deep insight for a control engineer to analyze the systems stability under different operating conditions. Using a modeled transfer function in both the time and frequency domains, this paper investigates the relative stability of the DC-to-DC boost converter. The circuits produced output responses under various operating situations after being simulated in MATLAB. The output waveforms of both ideal and non-ideal boost dc-dc converter circuits were carefully examined using established techniques such as the Nyquist stability criteria, the Bode method, and the Root locus approach. The system is evidently keeping within stable bounds for duty cycles below 50% and moving into unstable regions for duty cycles over 50% based on the root locus, bode, and Nyquist plots. With this approach, the transfer function, output waveforms, and overall stability of the DC-DC boost converter circuit are more thoroughly understood. By modifying lumped bounds L, C, R, RL, and RC and assessing other obligation cycle k attributes, more research into the optimal scenario for the most extreme rise may be completed.

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