Efficient Design and Implementation of Low-Power 1-Bit Full Adder for VLSI Applications

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ABSTRACT:

This paper describes the design of two efficient 1-Bit full-adder cells that operate at high speeds while consuming low power. These cells utilize an unconventional internal structure and employ a both Pass-Transistor (PT) logic and Transmission gate logic styles, resulting in a condensed power-delay product (PDP). In order to assess their performance, we conducted a comparative analysis of these full-adders with alternative designs recognized for their minimal power-delay product (PDP) in terms of speed, power consumption, and area. The 1-bit full-adders were fabricated using a 0.25-µm CMOS technology and underwent extensive testing using a comprehensive test bench. The test bench facilitated the measurement of both the input current drawn from the 1-bit full-adder and the current supplied from the control source. Based on pre-layout simulations, our proposed 1-Bit full-adders have shown superior performance compared to their counterparts. Specifically, they exhibit an average advantage of 80% in terms of power-delay product (PDP), indicating improved efficiency in balancing power consumption and speed. Furthermore, these full-adders occupy only 40% of the relative area, indicating a more compact and space-efficient design. The performance evaluation of the proposed 1-bit adder circuit was conducted using Mentor Graphics Schematic Composer. The simulations were carried out with a single-ended supply voltage of 5 V, utilizing the model parameters of a TSMC 0.25-µm CMOS technology.

INTRODUCTION:

The constant drive for faster and more efficient digital systems has led to extensive research on improving the design and performance of 1-bit full adder cells. These cells serve as critical components in arithmetic circuits, influencing the overall speed, power consumption, and area utilization of the system [1]. As a result, the development of optimized full adder designs is crucial for advancing the state-of-the-art in high-performance arithmetic circuits [2].

In recent years, numerous full adder cell designs have been proposed in the literature, each aiming to address specific challenges and optimize different aspects of the circuit. These designs employ a variety of logic styles, transistor configurations, and circuit topologies to achieve improved performance metrics such as propagation delay, power consumption, and area efficiency [3].

This comparative analysis aims to evaluate and compare the performance of several prominent 1-bit full adder cell designs proposed in research journals. The study focuses on key metrics such as power-delay product (PDP), area utilization, and performance trade-offs [4]. By comprehensively examining these designs, we aim to provide valuable insights into the strengths and weaknesses of each approach, enabling designers to make informed decisions when selecting a suitable full adder cell for their specific requirements [5].

The comparative analysis encompasses a diverse range of full adder cell designs, including transmission gate-based adders, GDI-based adders, hybrid adders, and majority function-based adders. Each design is carefully analyzed and evaluated using state-of-the-art simulation tools and metrics to provide a comprehensive and objective assessment [6]-[7].

The remainder of this paper is organized as follows: Section 2 provides an overview of the related work and existing full adder cell designs. Section 3 presents the methodology and implementation of proposed adder cell. Section 4 discusses the simulation results and performance metrics obtained from the simulations. Finally, Section 5 concludes the paper with summary and key findings.

State of the Art:

There are several existing 1-bit full adder designs, each with its own trade-offs in terms of performance, area, power consumption, and other design considerations [8].Arithmetic circuits play a vital role in numerous digital systems, such as microprocessors, digital signal processors, and arithmetic logic units [9]. The fundamental building block of these circuits is the 1-bit full adder, responsible for adding two binary digits along with a carry-in to produce the sum and carry-out [10]. The efficiency and performance of arithmetic circuits heavily rely on the design and implementation of these 1-bit full adder cells. Therefore, there is a growing interest in exploring and analyzing various full adder cell designs to identify the most suitable options for high-performance applications [11].

Several standard implementations for the 1-bit full adder cells as follows:

Conventional CMOS full adder circuit:

The depicted conventional CMOS full adder cell in Figure 1 is composed of 28 transistors, as stated in reference [12]. In the realm of logic design, there exist multiple logic styles that can be explored, with each style emphasizing specific performance metrics while potentially compromising others. As a result, the development of a cell library is influenced by different design constraints dictated by specific applications. This ensures that the library caters to the diverse needs and requirements of various design scenarios.For instance, the static logic approach is known for its robustness against noise, which ensures reliable operation even in the presence of disturbances.However, achieving ease of design is not always a straightforward task. While the CMOS design style is known for its robustness, it may not be the most area-efficient option for complex gates with large fan-ins. The CMOS design style typically requires a larger number of transistors to implement complex logic functions, which can increase the overall area occupation. Therefore, careful consideration is necessary when selecting a static Structure for realizing logic functions, taking into accounts both robustness and area efficiency trade-offs.

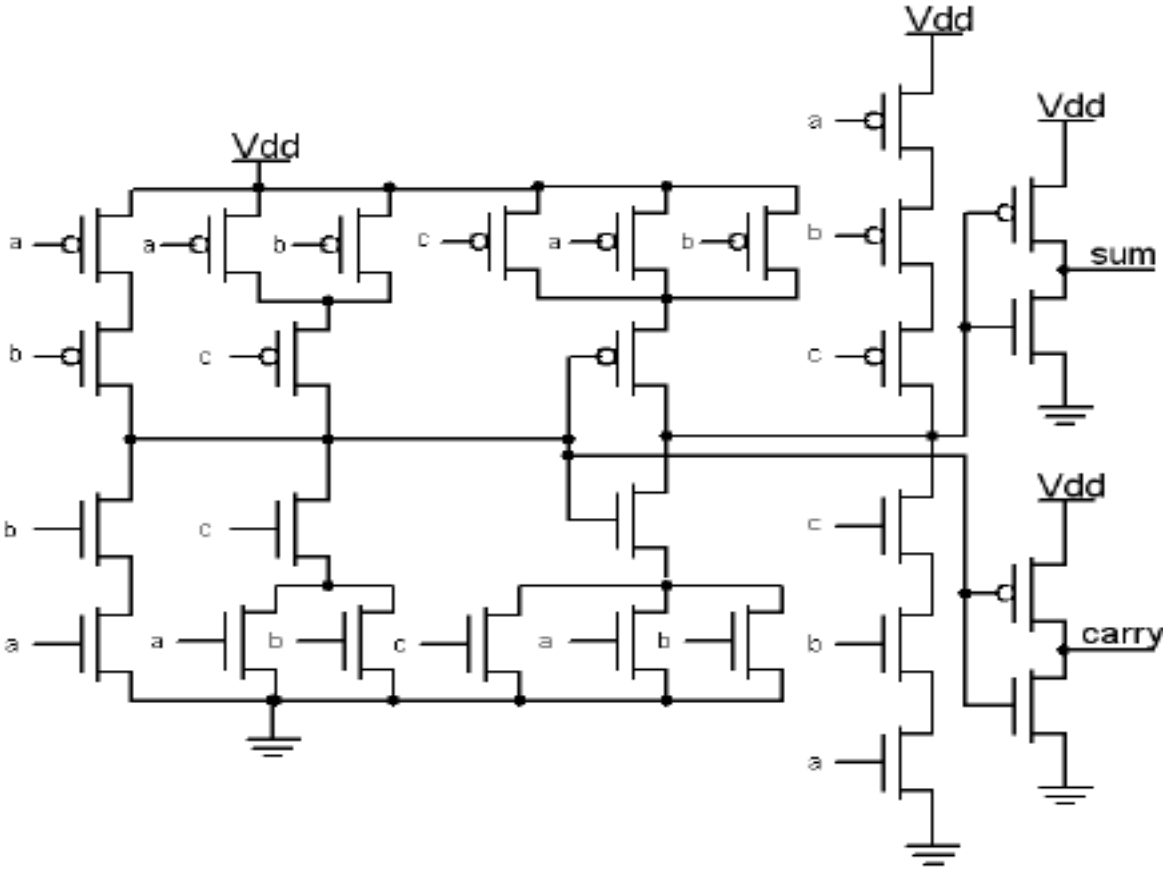

Fig 1: Conventional CMOS Full Adder Circuit Diagram

Complementary Pass Transistor Logic (CPL):

Complementary Pass Transistor Logic (CPL) utilizes the concept of pass transistors to perform logic operations. In the context of a 1-bit full adder operation, CPL employs pass transistors to achieve the addition of two 1-bit binary numbers while minimizing power consumption and area overhead. This approach involves the strategic arrangement and control of pass transistors to facilitate efficient computation of the sum and carry-out signals, essential components of the full adder operation, utilizes a dual-rail construction consisting of 32 transistors [12].

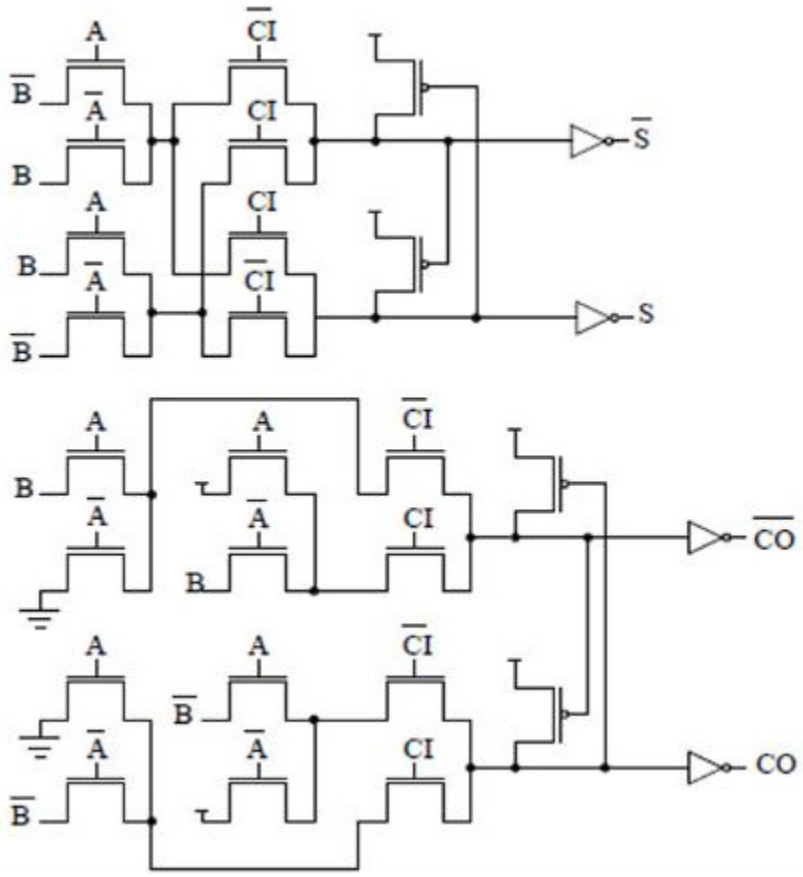

Fig 2. CPL Full Adder Implementation

CPL is not typically favored for low-power applications due to several factors. Firstly, its high transistor count significantly contributes to increased power consumption. Additionally, the high switching activity observed at intermediate nodes within CPL circuits further exacerbates power consumption. Moreover, the inputs of CPL circuits can become overloaded, leading to inefficiencies in operation. These combined drawbacks make CPL less suitable for low-power designs compared to alternative logic families.

Transmission-Gates CMOS (TG-CMOS):

TG-CMOS involves utilizing transmission gates in CMOS logic circuits. In the context of a 1-bit full adder operation, TG-CMOS employs transmission gates to facilitate the addition of two 1-bit

binary numbers. This approach offers advantages such as reduced transistor count, improved speed, and lower power consumption compared to traditional CMOS implementations. By strategically integrating transmission gates into the circuit design, TG-CMOS achieves efficient computation of the sum and carry-out signals necessary for accurate addition while optimizing performance metrics as portrayed in Figure 3 [13]. TG-CMOS full adders leverage transmission gates within CMOS logic circuits. This approach results in reduced transistor count, simpler circuitry, and lower power consumption compared to conventional CMOS designs. Moreover, TG-CMOS full adder exhibit improved speed and reduced propagation delays due to the more direct routing of signals through transmission gates. Furthermore, TG-CMOS full adders tend to exhibit a lower transistor count compared to conventional CMOS full adders due to the simplified circuitry enabled by the use of transmission gates. This reduction in transistor count can contribute to benefits such as reduced power consumption, improved speed, and potentially lower manufacturing costs.

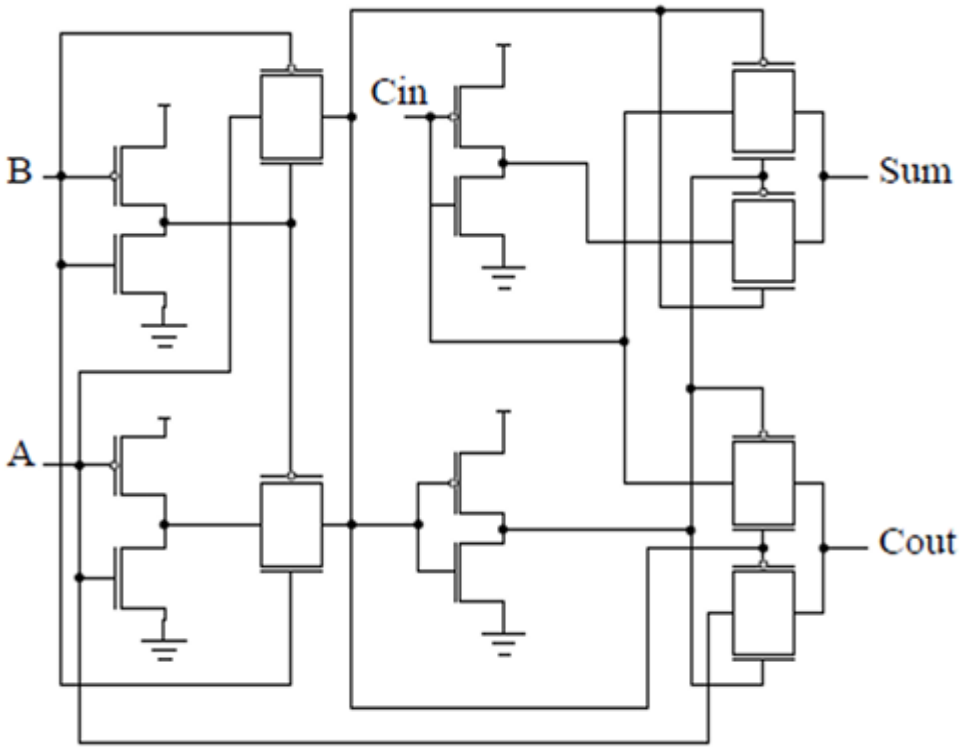

Fig 3.TG-CMOS Full Adder Implementation

Therefore, TG-CMOS full adders present a more efficient and potentially more cost-effective alternative with reduced power consumption, simpler circuitry, and improved performance characteristics.

BLOCK DIAGRAM:

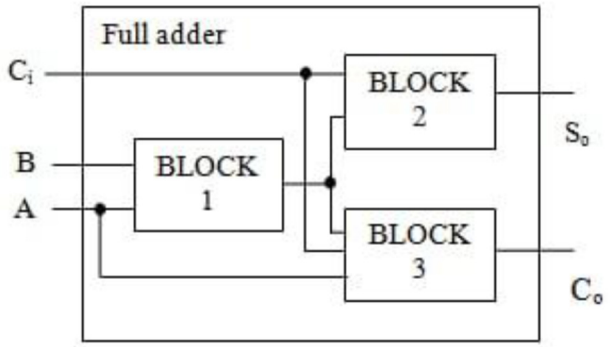

Fig 4.Block diagram of proposed 1-bit adder cell

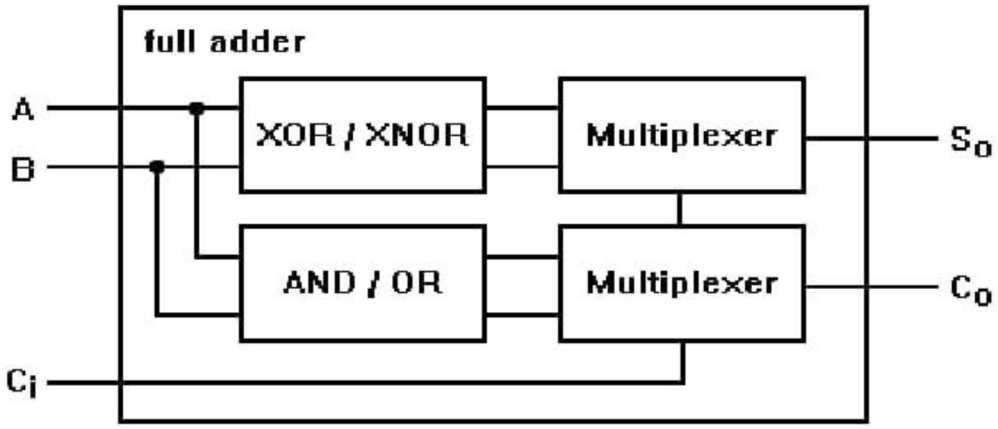

Fig 5. Schematic Structure of proposed 1-bit adder cell

The configuration depicted in Fig.2 has emerged as the predominant structure for numerous advancements in the evolution of the 1-bit full-adder module. These cells employ an alternative internal logic structure, incorporating both pass-transistor logic and Transmission gate logic styles. This configuration consists of three main logical blocks within the adder module: an XOR-XNOR gate responsible for obtaining A XOR B and A XOR B (Block 1), along with XOR blocks or multiplexers utilized to derive the SUM (So) and CARRY (Co) outputs (Blocks 2 and 3). A thorough proportional scrutiny was conducted with the goal of identifying the most effective implementation for Block 1. An essential finding from this study emphasized a significant concern regarding propagation delay in a full-adder utilizing the logic structure illustrated in Fig. 4.The challenge arises from the need to produce both the A XOR B signal and its complement as transitional signals, which are subsequently utilized to drive other blocks for generating the final outputs.

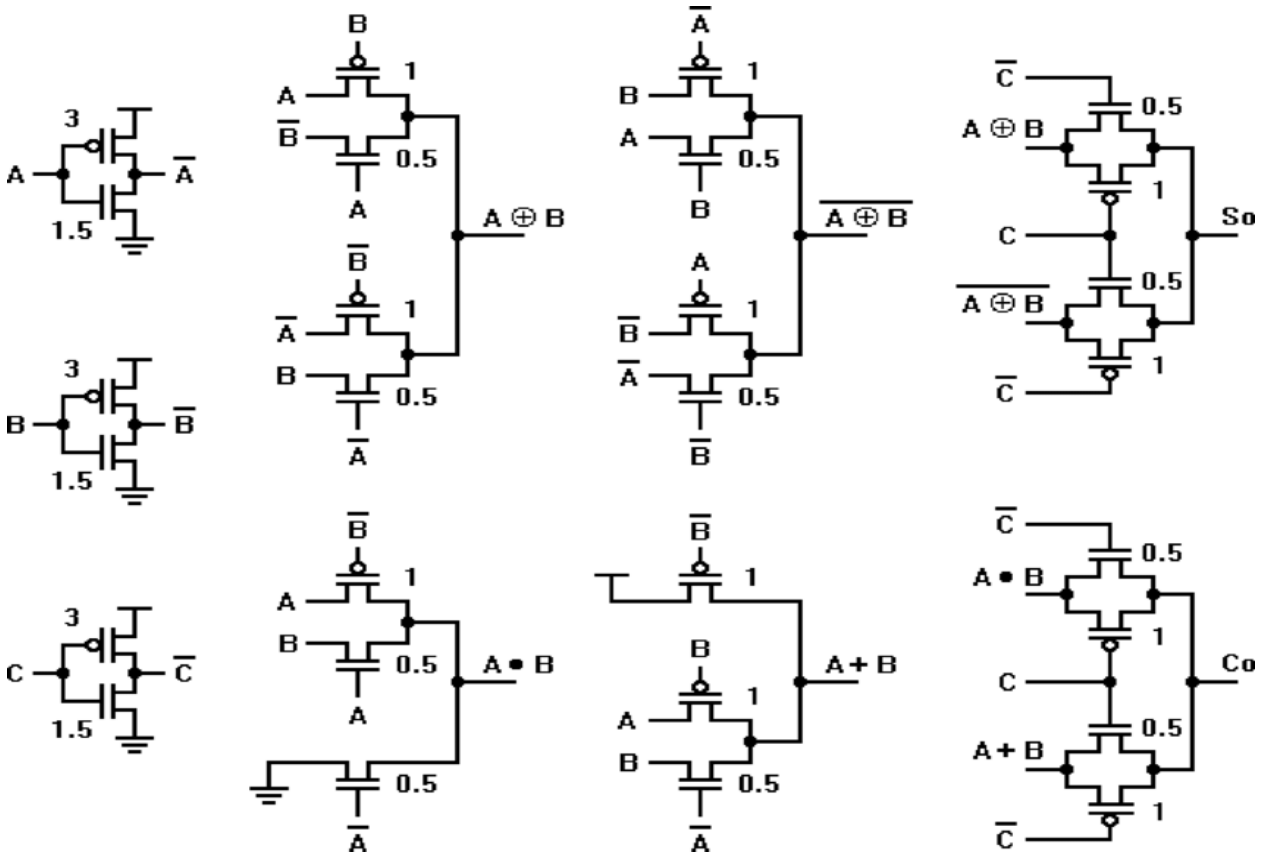

Fig 6: Proposed 1-Bit Full Adder1 Circuit Diagram using Hybrid Logic

Hence, the total propagation delay and, in many instances, power consumption of the 1-bit full-adder are contingent upon the delay and voltage swing of the A XOR B signal and its complement, which are generated within the cell. To improve the operational speed of the full-adder, it is necessary to develop a new logic structure that eliminates the need for generating intermediate signals to control the selection or transmission of other signals along the critical path. Due to the finite slopes and diminished voltage swing of the full-adder output signals, it is vital to take into version to short-circuit and static consumption of inverters connected to the outputs of the Device under Test (DUT).Incorporating the effects and power consumption of buffers connected at the inputs and outputs of the DUT is crucial, considering that the DUT is consistently utilized alongside other devices to construct larger systems. The static inverters serve as a generalization across various operating scenarios. Test input patterns recommended in utilized for stimulus vectors, encompassing all required input combinations to ascertain worst-case propagation delay and power consumption values.

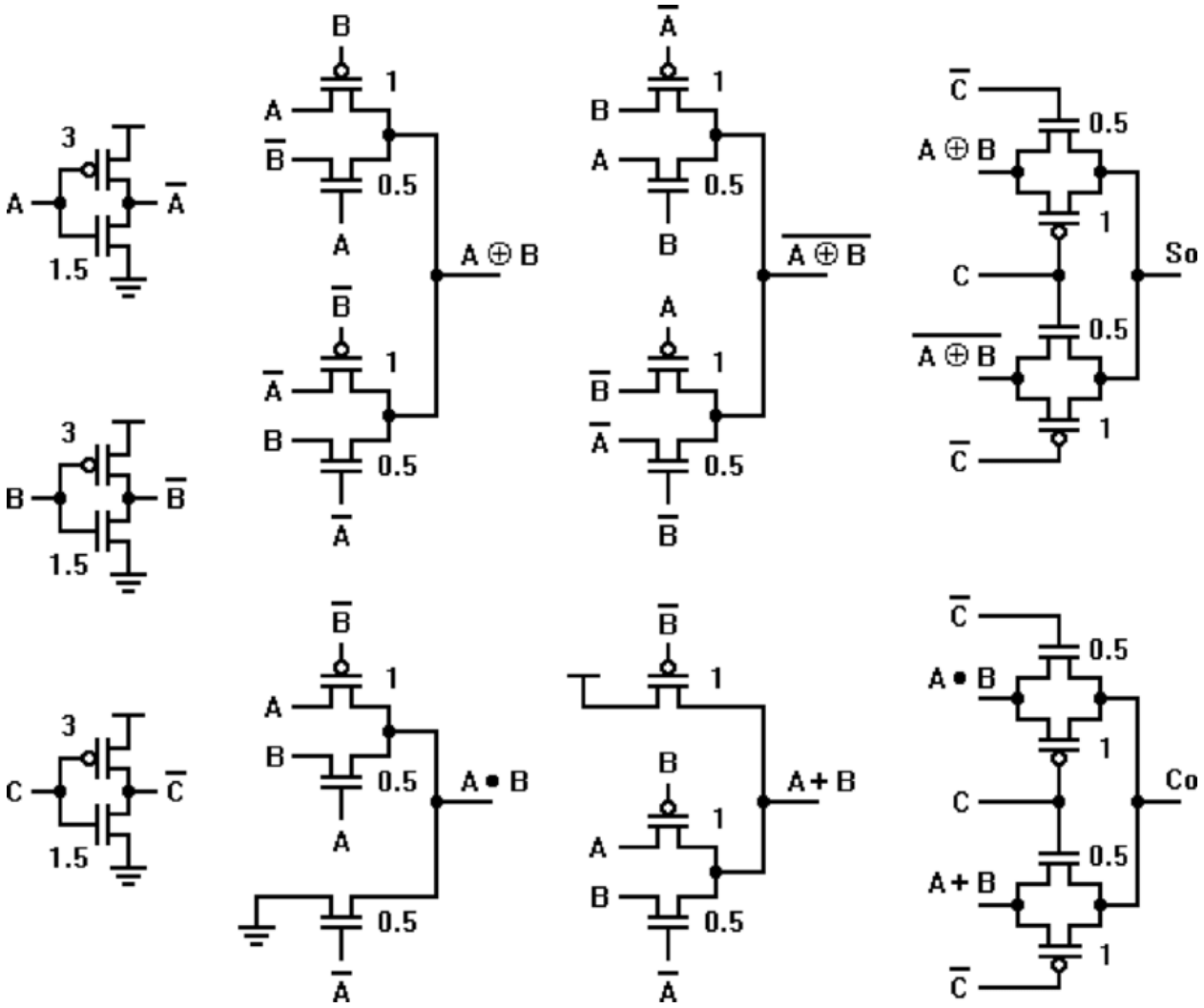

Fig 7:Proposed 1-Bit Full Adder2 Circuit Diagram using Hybrid Logic

Expanding on the findings, two novel full-adders were developed utilizing the Dynamic Pseudo NMOS Logic (DPL) and the Source-Coupled Pass Transistor Logic (SR-CPL) styles, in conjunction with a novel logic architecture depicted in Figure 5. Figure 6 showcases a full-adder crafted with the DPL logic style to fabricate the XOR/XNOR gates, complemented by a pass-transistor-based multiplexer to generate the sum output. In contrast, Figure 7 demonstrates the utilization of the SR-CPL logic style in constructing these XOR/XNOR gates.

In both cases, the AND/OR gates were assembled employing a pass-transistor configuration devoid of power and ground connections, for AND, OR functions, respectively. Additionally, a pass-transistor-based multiplexer was incorporated to derive another output. The dimensions of the input buffers led to a certain level of deterioration in the input signals, whereas the output buffer size was tailored to accommodate the load of four small inverters specific to this technology. The test bed provides a comprehensive representation of static CMOS gates both driving and being driven within the full-adder cell under examination.

An essential feature of this simulation environment is its incorporation of various power components, including the dynamic aspect. A comparison was conducted on the performance of five full-adders Convention CMOS Full Adders (28T), CPL Logic (32T), TG-CMOS (14T) logic. The schematics and layouts were designed using TSMC's 0.25-micrometer CMOS technology and simulated using Mentor Graphics. Post-layout extracted net lists were utilized, which incorporated parasitic elements.

The performance evaluation of the proposed 1-bit adder circuit was conducted using Mentor Graphics Schematic Composer, employing a single-ended supply voltage of 5 V and model parameters corresponding to TSMC's 0.25-micrometer CMOS technology. To ensure an equitable comparison, transistor sizes for each 1-bit full-adder were sourced from the respective papers. Static dissipation was observed exclusively in two full-adders, namely new14T and CPL. The design of these adders utilized logic styles characterized by incomplete voltage swings within specific internal nodes, thereby contributing to this aspect of power consumption.

Simulation Results:

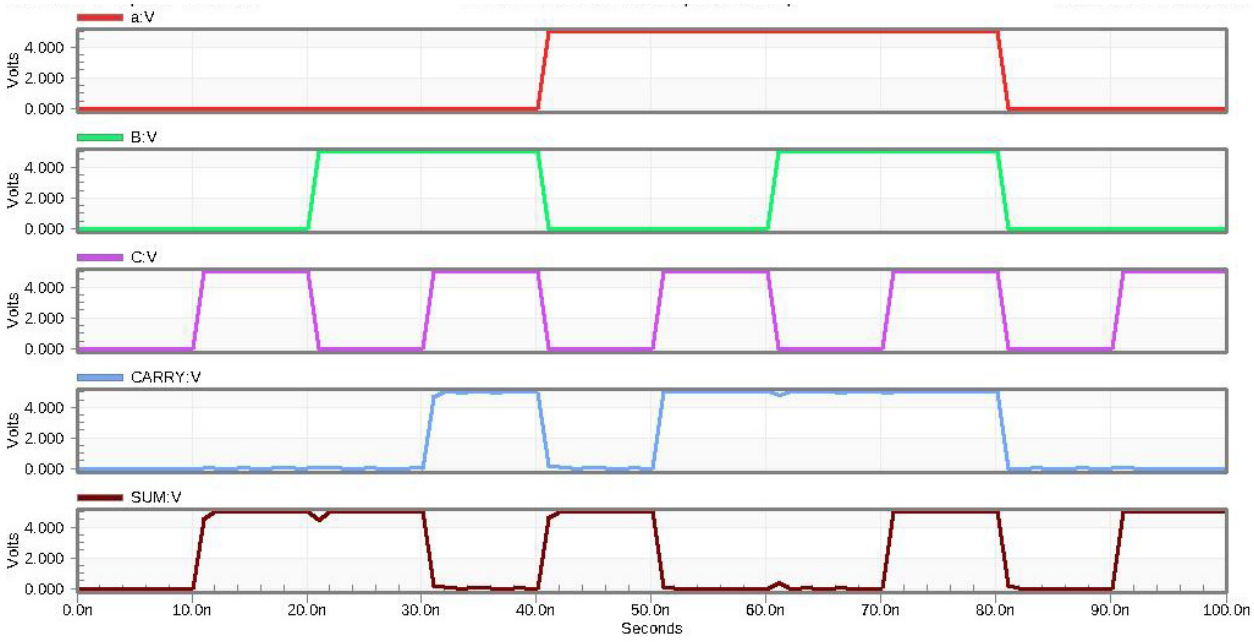

Fig 8: Simulation outcome for Proposed Structure1 Schematic 1

Simulation Outcomefor Proposed Structure1 Schematic& Proposed Structure 2 Schematic as shown in figure 8 &9 from the inputs of 1-bit full adder using hybrid logic.

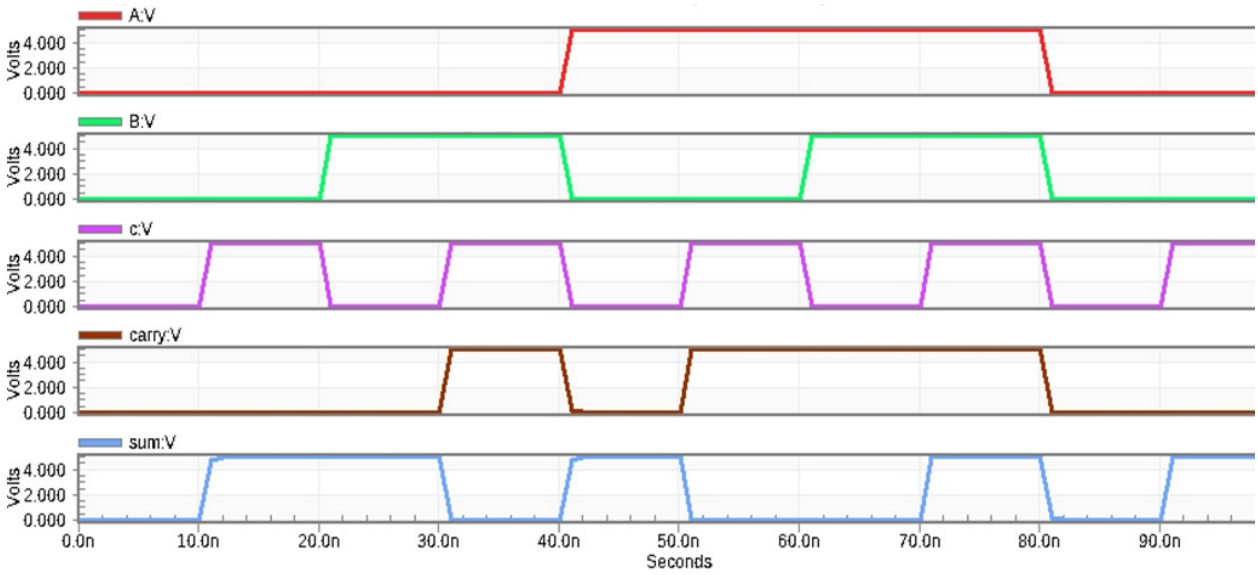

Fig 9: Simulation outcome for Proposed Structure2 Schematic

Table 1 in this study presents a performance comparison between the proposed implementation of 1-bit full adder cells and alternative implementations. Notably, among the alternatives, Proposed Full Adder 2 outperforms the all the adder cells, exhibiting a superior power-delay product.

Table 1 presents performance comparisons and pre-layout simulation results of both the proposed and alternative implementations of 1-bit full adder cells. These simulations were conducted under a supply voltage (V_{dd}) of 5 V, utilizing 0.25-micrometer CMOS technology.

Design	Power(µW)	Delay (Ps)	PDP (fJ)
CMOS [12]	10.254	324.52	3.327
CPL [12]	12.837	213.85	2.745
TGA [13]	11.944	316.83	3.784
Proposed Full Adder 1	**8.562**	**234.67**	**2.009**
Proposed Full Adder 2	**7.846**	**247.84**	**1.944**

CONCLUSION:

An alternate approach has been proposed for the design of 1-bit full-adder cells, presenting a narrative proposed Schematic structure using hybrid logic. This new structure offers an alternative solution to the existing designs. To demonstrate the advantages of the narrative

proposed Schematic structure, two full-adders were developed using TG-CMOS & PTL. These designs were implemented utilizing TSMC 0.25-μm CMOS technology. Subsequent simulations and comparisons were carried out in comparison to recently reported energy-efficient full-adders. Through simulations conducted using Mentor Graphics Schematic Composer, significant findings were observed. The proposed full-adders demonstrated a remarkable area utilization of only 40% when compared to the largest full-adder in the comparison set. This highlights the efficiency and versatility of the narrative proposed Schematic structure in terms of both area utilization and power-supply voltage optimization. For remarkable power savings up to 80% and speed enhancements up to 25%. These improvements were achieved by jointly optimizing the design, resulting in an impressive 85% reduction in Power-Delay Product (PDP).

During our evaluation, we conducted an analysis of the maximum operating frequency for each full adder under a 5 V power supply. The proposed full-adders demonstrated an impressive peak frequency of up to 1.25 GHz, positioning them as the second-highest performers in terms of frequency, surpassed only by the CPL cell. This highlights the strong frequency capabilities of the proposed full-adders within the context of the comparison set. However, it is important to note that this increase in frequency was accompanied by a noticeable rise in power consumption and area requirements compared to the other designs. The improvements in power consumption for the full-adders were organized in descending order, aligning with the reported optimizations outlined in their respective papers. This systematic arrangement allowed for a clear understanding of the magnitude of power savings achieved by each full-adder design, providing valuable insights into the effectiveness of the proposed optimizations.

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