A Soft-Switched Topology for Improved Efficiency in Three-Level PWM Voltage Source Inverters

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***Abstract*—The conventional H-Bridge inverter topology has long been recognized for its limited efficiency and power density. In response to these challenges, this study introduces a unique approach to achieving soft-switching, a technique renowned for enhancing operational efficiency and power density. Unlike existing methodologies that necessitate additional switches, the proposed design leverages only two supplementary switches compared to the standard H-Bridge inverter. The paper explores the intricacies of this novel topology, conducting a comprehensive analysis of the proposed topology and loss analysis. To validate the efficiency of the proposed concept, a 1 kW single-phase inverter model was simulated using MATLAB/Simulink. The outcomes of the simulations unequivocally demonstrate the superior performance of this new design in comparison to the traditional H-Bridge topology, particularly in terms of efficiency.**

***Index Terms*—Soft-switching, Zero Voltage Switching (ZVS), Zero Current Switching (ZCS), PWM, Loss Analysis.**

I. Introduction

Voltage source inverters are commonly used for power generation, motor drives, and other applications due to their versatility. [1]. The industry is moving toward increasing the power density of converters, which can save money by using less physical material and components in the creation of commercial inverters [2]. To improve the power density of the inverter, it is advisable to operate the inverter at a higher switching frequency, which leads to a reduction in the reactive filter requirement of the converter [3]. An increment in switching frequency leads to an escalation of switching losses, thereby compromising the overall efficiency of the power inverter. The maximum switching frequency of commercial IGBT-based inverters is typically 20 kHz [4].

To address the prior issue in the development of high-frequency inverters, it is possible to employ soft-switching techniques to enhance the power density of the inverter while simultaneously achieving high levels of efficiency. Extensive studies have been conducted in academic journals regarding the attainment of soft switching for inverter switches through the utilization of the ZVS or ZCS condition [5] and [6]. This can be categorized into two main components resonant DC-Link and resonant AC-Link.

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In 1989, Divan introduced the idea of a resonant DC-link (RDCL) soft-switching inverter (Divan, 1989). In this, a resonant tank links between the DC-link and inverter switches, providing a momentary zero voltage condition By switching the inverter switches in these specific instances, it is feasible to reduce power losses, but it also offers the problem of high voltage stress, and integral pulse density modulation is applied to enable soft switching. A paper on the resonant DC-link inverter [13] identified that these kinds of circuits are inhibitory for PWM approaches due to their absence of a function that allows for a continuous variation in the pulse width. To face this difficulty, certain changes in the resonant DC-link inverter are present in active clamped resonant DC-link and quasi-resonant DC-link inverters [8] - [10].

The quasi-resonant soft-switching topology employs classic PWM control principles while introducing additional circuitry to create zero-voltage switching (ZVS) conditions for the inverter switches. This solution offers a dedicated DC-link switch that isolates the input power source from the inverter's switches. Additionally, a resonant capacitor is inserted in parallel with the DC-Link. When a commutation event (change of state) becomes essential for the inverter switches, the DC-link switch is disconnected. Thus, the resonant capacitor discharges through a dedicated auxiliary circuit, simplifying the transition of the inverter switches under ZVS conditions [12] and [17]. During commutation, AC-side soft-switching topologies introduce an additional resonant network to permit zero-voltage turn-on (ZVT) for the inverter switches. [15] presents an auxiliary resonant commuted pole (ARCP) approach that involves three half-bridge circuits coupled in series with resonant inductors at the load terminals. During the switching transition, a resonance state is formed between these inductors and the output capacitance of the inverter switches, allowing ZVT operation. However, this approach involves a large increase in component count, making it more suitable for high-power, three-phase inverter.

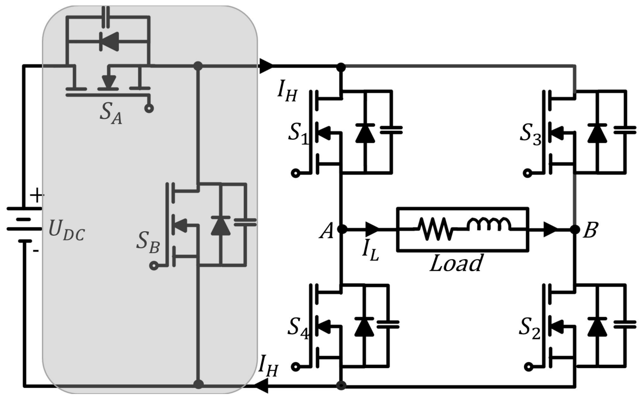

Fig. 1. Proposed topology

In [20] offers a unique generalized topology that considerably reduces component count while preserving high efficiency and ZVS capabilities for a two-level voltage source inverter Author would like to introduce this topology and validate this topology for a three-level voltage source inverter.

The rest of the paper is organized as follows Analysis of the proposed topology is present in section II, parameter design inverter is present in section III. while section IV focuses on the simulation and result validation.

II. ANALYSIS OF PROPOSED TOPOLOGY

To demonstrate the functionality of the proposed topology, a three-level single-phase VSI is deployed as a demonstration platform. A key component of this proposed design is an auxiliary circuit positioned strategically between the DC-Link and the VSI input, as depicted in fig.1. This specific area has two auxiliary switches, indicated as S_A and S_B, which enable the soft-switching of the inverter.

The turn-off process commences by disconnecting switch S_A. This action enables the load current to pass through the auxiliary path constructed by activating switch S_B. The flow of this current, together with the conduction of the body diode, permits zero voltage switching (ZVS) for switches S_1 and S_2 consequently resulting in a further reduction of losses.

The process of commutation exclusively employs active switches, hence reducing the demand for bulky and delicate passive components such as inductors and capacitors. This feature endows it with inherent versatility and robustness, ensuring successful functioning irrespective of load changes or types.

A. operation of proposed converter

The steady-state operating principle of the proposed topology is categorized into six modes, namely modes I to VI, as illustrated in fig.2. Correspondingly, the operating waveform can be observed in fig.3.

1) Mode 1- ($t_0 \leq t_1$): This mode is initiated when S_A is activated under a zero current condition. The load voltage is established at $+U_{DC}$, Subsequently, the load current gradually increases from zero to its maximum value, which is dictated by the particular characteristics of the load. This operational state is commonly known as "Active Mode." Figure 2(a) shows an arrowhead that indicates the current's direction. The switches' instantaneous current and voltage characteristics are presented as follows:

$I_{Sw1} = I_{Sw2} = I_{S_A} = I_H = I_L$,

$U_{AB} = +U_{DC}$, $U_{SW1} = U_{SW2} = U_{SA} = 0$, $U_{SW3} = U_{SW4} = +U_{DC}$.

2) Mode 2 - ($t_1 \leq t_2$): After time instant t_1, the DC-link switch S_A is turned off under hard switching. Consequently, the load currently experiences a current path disruption. Diode D_{SB} serves as a freewheeling channel for the aforementioned current, as depicted in fig 2(b). The voltage potential between points A and B is zero. The instantaneous current and Voltage characteristics of the switches are shown as follows:

$I_{Sw1} = I_{Sw2} = I_H = D_{SB} = I_L$,

$U_{AB} = 0$, $U_{SW1} = U_{SW2} = U_{SB} = 0$.

3) Mode 3 - ($t_2 \leq t_3$): Before time instant t_2, the diode D_{SB} commences conduction, facilitating the switch S_B to be triggered in the ZVS. subsequently, the load current is trying to complete its course through the switch S_{SB}. Fig.2(d) indicates the flow direction of the current. The voltage drop across switch S_B, which is ideally zero and practically one or two volts, is equal to the voltage between switches U_{SW1} and U_{SW2} at instant t_5. As such, switch S_1 and switch S_2 are both turned off at this voltage level. The voltage potential across points A and B is zero. The instantaneous current and voltage characteristics of the switches are given as follows:

$I_{Sw1} = I_{Sw2} = I_{SB} = I_H = D_{SB} = 0$,

$U_{AB} = 0$, $U_{SW1} = {}_{SW2} = V_{SB} = 0$.

4) Mode 4 - ($t_3 \leq t_4$): After time instant t_3, the inverter switch S_1 and S_2 turn-off. The load current is trying to complete its path via the diode D_{S3} and D_{S4}. Fig.2(d) depicts the flow direction of the current. The voltage potential across points A and B is zero. The instantaneous current and voltage characteristics of the switches are described as follows:

$I_{SB} = I_{DS_4} = I_{DS_3} = I_{SB} = I_H = I_L$,

$U_{AB} = 0$, $U_{SW1} = U_{SW2} = U_{SB} = 0$.

5) Mode 5 - ($t_4 \leq t_5$): Before instant t_4, the diodes D_{S3} and D_{S4} commence conduction, causing the switches S_1 and S_2 to be turned on in the ZVS. Now free-wheel current tries to complete its path through the switch S_{SB}. Fig.2(e) illustrates the flow direction of the current and switch S_B. At the end of this mode, the instantaneous voltage and current of the switches are as follows:

$U_{MN} = 0$, $U_{SA} = U_{DC}$,

$I_{Sw1} = I_{Sw2} = I_{SB} = I_H = I_L$.

6) Mode 6 - ($t_5 \leq t_6$): After instant t_6, if the free-wheeling current is not zero, the switch S_B will be turned off under hard-switch. In this scenario, the free-wheeling current attempts to find its path through the diode D_{SB}. Fig.2(f) illustrates the flow direction of the current. At the end of this mode, the instantaneous current and voltage of the switches are as follows:

$I_{Sw3} = I_{Sw4} = I_H = I_L$,

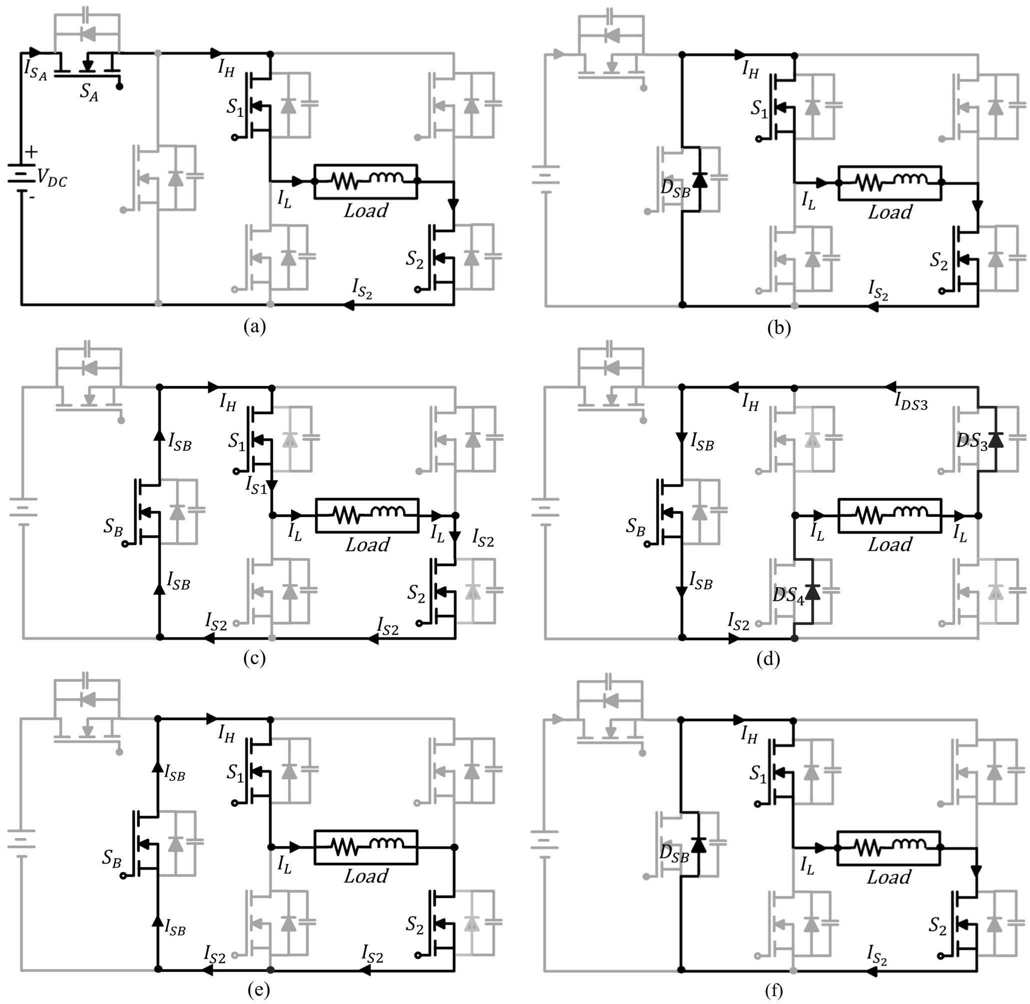

Fig. 2. operating modes of proposed topology

U_{AB} = 0, $U_{SW3} = U_{SW4} = \frac{U_{DC}}{4}$, $U_{SB} = V_{DC}$, $U_{SA} = U_{SB} = \frac{V_{DC}}{2}$.

III. Power-loss Model

The losses in the three-phase inverter can be categorized into power semiconductor losses and ohmic losses. The power semiconductor losses can be further divided into switching losses and conduction losses.

$$P_{Total} = P_{Cond} + P_{SW} \tag{1}$$

The semiconductor device experiences average total power losses denoted as P_{Total}, average switching losses denoted as P_{SW}, and average conduction losses denoted as P_{Cond}.

A. Switching loss

The power losses of the semiconductor devices are analyzed using different power loads. The semiconductor power device losses are divided into conduction and switching losses. The switching losses can be divided into Switch-ON losses and Switch-OFF losses.

The semiconductor power device losses are explained and derived in detail in [17]. Fig.4 and Fig.5 illustrate the switching energies involved during Turn-on and Turn-off transitions. I_{DS} represents the current flowing through the switching device, tri represents the rise time of the current, tru represents the rise time of the voltage, tfi represents the fall time of the current, and tfu represents the fall time of the voltage.

The switching losses depend on both the switching energy and the switching frequency of the device. The switching energy, in turn, relies on the device's junction temperature, the voltage across the device during switching, and the final current passing through the device. The switching loss of a MOSFET is now determined by the energy loss within a specific time interval, which is calculated as the sum of the rise time of current (tri) and the time for the MOSFET to fall voltage (tfu). The values of tri and tfu are calculated [18]. Energy loss calculation for turn on and turn off transient is given below:

$$E_{ON} = \int_0^{t_{ri}+t_{fu}} V_{DS} I_{DS} \ dt \tag{2}$$

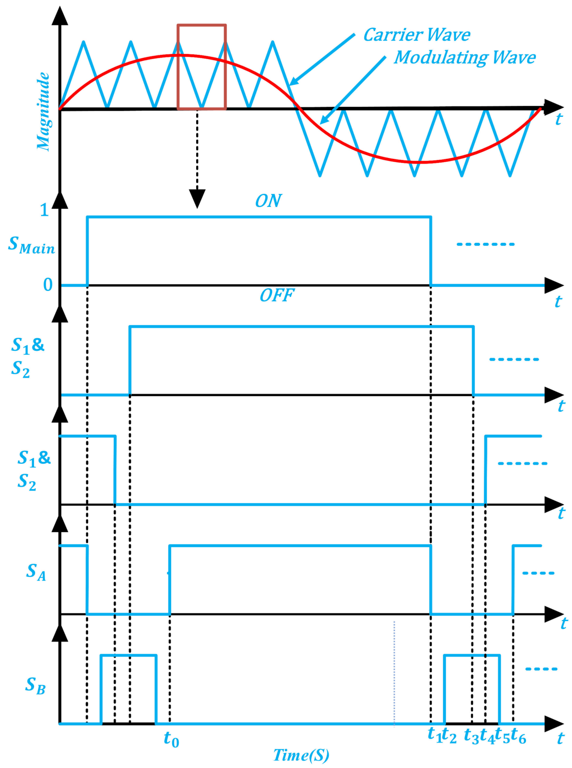

Fig. 3. Operating Waveform

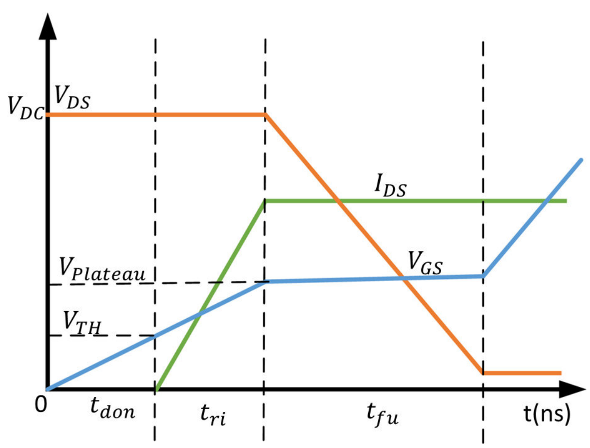

Fig. 4. Turn-ON transient

$$= \frac{1}{2} V_{DS} I_{DS} (t_{ri} + t_{fu}) \tag{3}$$

The average value of E_{ON} during the sinusoidal period inverter output current also varies in a sinusoidal fashion.

$$= \int_0^{\pi} \frac{1}{2} \times V_{DS} \times I_{DS}(t_{ri} + t_{fu}) \tag{4}$$

$$= \frac{1}{\sqrt{2}\pi} \times V_{DS} \times I_{DS}(t_{ri} + t_{fu}) \tag{5}$$

Additionally, there is another part of energy loss included in MOSFET turn-on energy loss is caused by the anti-parallel

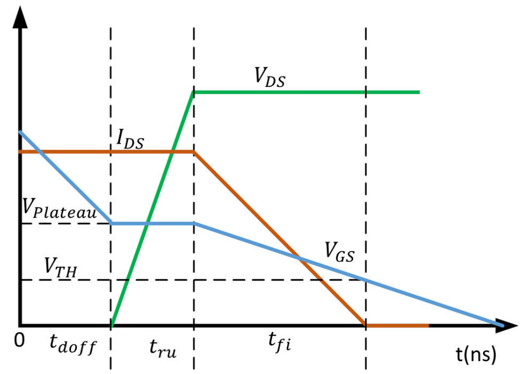

Fig. 5. Turn-off transient

body diode reverse recovery current on the calculations from data-sheet parameter value of $t_{ri} = 5.89 \times 10^{-8}$, $t_{fu} = 6.99 \times 10^{-6}$,$Q_{rr} = 9 \times 10^{-6}$.

Taking this part of energy losses into account,E_{ON} can be given by:

$$E_{ON} = \frac{1}{\sqrt{2}\pi} \times V_{DS} \times I_{DS}(t_{ri} + t_{fu}) + Q_{rr} \times V_{DC} \tag{6}$$

$$= \frac{1}{\sqrt{2 \times \pi}} 200 \times 9.09 \times [120 \times 10^{-9} + 7.09 \times 10^{-9}]$$
$$+ 9 \times 200 \times 10e^{-}9$$
$$= 1.63 \times 10^{-3}$$

After that MOSFET turnoff energy loss is estimated by a similar solution.

$$E_{OFF} = \int_0^{t_{ru} + t_{fi}} V_{DS} I_{DS} \, dt \tag{7}$$

The solution of the above equation number (11) is given by

$$E_{OFF} = \frac{1}{\sqrt{2}\pi} \times V_{DS} \times I_{DS}(t_{ru} + t_{fi}) \tag{8}$$

$$= \frac{1}{\sqrt{2 \times \pi}} 200 \times 9.09 \times [9.22 \times 10^{-8} + 98 \times 10^{-9}]$$
$$= 0.173 \times 10^{-3}$$

the calculation of MOSFET switching power losses is determined by the equation provided:

$$P_{SW} = (E_{on} + E_{off}) \times F_{SW} \tag{9}$$

$$= [(1.73 + 0.173) \times 10^{-3}] \times 10000$$

Approximate switching loss = $19.03W$ per MOSFET

B. Conduction loss

The voltage drop across MOSFET can be simplified as a resistor in the channel, while the voltage drop across diodes can be simplified as a voltage source in series with a resistor in the channel. These simplifications are represented by equations (10) and (11) respectively.

$$V_{DS} = I_{DS} \times R_{DS} \tag{10}$$

$$V_{AK} = V_{f0} + I_D \times R_{AK} \tag{11}$$

Where R_{DS} on-state resistance of the MOSFET, V_{AK} anode to cathode voltage of body diode of the MOSFET,V_{f0} Forward voltage drop and R_{AK} diode on-state resistance. Detailed expression of the conduction loss is given in. conduction loss of MOSFET and body diode is given below:

Conduction loss of MOSFET:

$$P_{Cond(MOSFET)} = R_{DS} \times I_M^2[(\frac{1}{8} + \frac{M \times \cos\phi 1}{3\pi})] \quad (12)$$

Conduction loss of DIODE:

$$\begin{aligned} P_{Cond(DIODE)} =& V_{fo} \times I_M \times [(\frac{1}{2\pi}) - \frac{M \times \cos\phi 1}{8}] \\ &+ R_{DS} \times I_M^2[(\frac{1}{8} - \frac{M \times \cos\phi 1}{3\pi})] \end{aligned} \quad (13)$$

where M is the Modulation Index, I_M Peak value of the output current,I_{RMS} root mean square value(RMS) of output current and $I_M = \sqrt{2} \times I_{RMS}$. To calculate the approximate conduction loss of the MOSFET and freewheeling diode, a simulation parameter is taken. M = 0.8, Forward voltage drop of body diode=1.5V, and $cos\phi 1 = 0.8$.

$$\begin{aligned} I_M &= \sqrt{2} \times 9.09 = 12.85A \\ P_{Cond(MOSFET)} &= 0.27 \times 12.85^2[\tfrac{1}{8} + \tfrac{0.8\times0.8}{3\pi}] \\ &= 8.65W \end{aligned}$$

$$\begin{aligned} P_{Cond(DIODE)} &= 1.5 \times 12.85 \times [(\tfrac{1}{2\pi}) - \tfrac{0.8\times0.8}{8}] \\ &+[0.27 \times 12.85^2(\tfrac{1}{8} - \tfrac{0.8\times0.8}{3\pi})] \\ &= 4.57W \end{aligned}$$

Approximate conduction loss of each MOSFET

$$\begin{aligned} &= P_{Cond(MOSFET)} + P_{Cond(DIODE)} \\ &= 8.65 + 4.57 = 13.22W \end{aligned}$$

For the H-Bridge inverter, four devices MOSFET in series are conducting current during the active states, while during the zero state the current flows through two devices MOSFET and two diodes. The low-frequency switching losses are neglected. Hence, the conduction and switching losses of the H-Bridge inverter can be given by:

$$P_{C\{loss\}} = 4(P_{C\{loss\}}(MOSFET)) \quad (14)$$

$$\begin{aligned} P_{C\{loss\}} =& 2(P_{C\{loss\}zero(MOSFET)} \\ &+ (P_{C\{loss\}zero(DIODE)}) \end{aligned} \quad (15)$$

$$P_{SW_{loss}} = 4(P_{SW_{on}} + P_{SW_{off}}) \quad (16)$$

In the given topology depicted in fig.2, three MOSFETs are responsible for conducting current during the active states. However, in the zero states, the current will bypass two devices and flow freely through another three MOSFETs and two diodes.

It is important to note that the low-frequency switching losses have been disregarded. Consequently, the losses incurred due to conduction and switching in the proposed topology can be expressed as follows:

$$P_{C\{loss\}} = 6(P_{C\{loss\}(MOSFET)}) \quad (17)$$

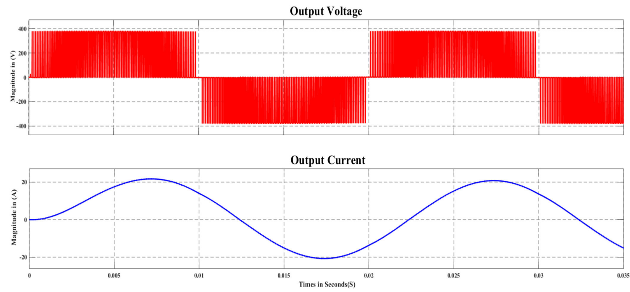

Fig. 6. Output Voltage and Current

$$\begin{aligned} P_{C\{loss\}} =& 2[P_{C\{loss\}\{zero\}(MOSFET)} \\ &+ (P_{C\{loss\}\{zero\}(Diode)})] \end{aligned} \quad (18)$$

$$P_{SW_{loss}} = 1(P_{SW_{on}} + P_{SW_{off}}) \quad (19)$$

The power losses in the proposed topology are evident, showcasing lower switching losses compared to the conventional H-Bridge. However, there is a slight increase in conduction losses.

IV. SIMULATION AND RESULT

The validation of the proposed converter topology working principle is carried out through modeling and simulation. The simulation of the proposed topology is performed using principal components in MATLAB/Simulink, as shown in fig.1, and table I.

In this simulation, an ideal DC source is connected in series with a wire resistor nΩ and a wire inductor nH. MOSFET switches from the Specialize Power System Library are utilized to simulate the H-bridge section of the DC-AC inverter, which has a resistance of 0.27 Ω and a capacitance of 350 pF as a snubber.

To verify the functionality of the topology inverter running at a modulation index of 0.8 and a switching frequency of 10kHz, a load resistor and an inductor of 10Ω and 1mH respectively, are connected on the load side. The simulations employ a Unipolar (PWM) technique. Fig.6 depicts the voltage and current output of the inverter.

Fig. 7 illustrates the ZVS turn-on of the MOSFET switch, with the current following a specific pattern. It rises when the gate pulse is triggered and returns to zero just before the gate pulse reaches zero. This mechanism enables the achievement of ZVS. Consequently, these switches S_1 to S_4 are controlled by this ZVS, making it the suggested converter that maintains ZCZVS switching throughout the cycle.

On the loss calculations, it is found that the H-Bridge topology has a total of 52.88W and 79.11W of conduction and switching losses, respectively. For the proposed topology, it is found that it has a total of 28.01W and 16.01W of conduction and switching losses, respectively. Note that loss in the auxiliary circuit is included in the proposed topology.

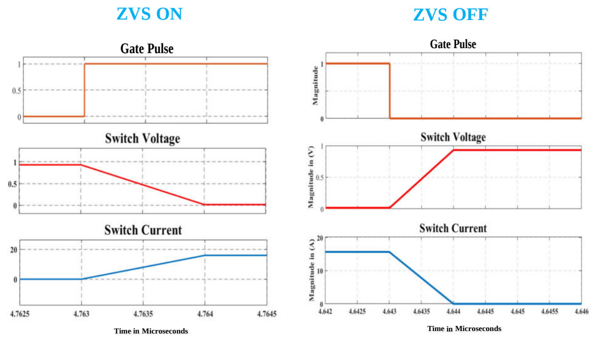

Fig. 7. Soft switching validation of proposed topology

TABLE I
SIMULATION PARAMETERS

Parameters	Values
Rated Power	1kW
DC link voltage	200V
DC link capacitor	832μF
Switching frequency	10kHz
MOSFET for the conventional H-Bridge Inverter	IRFP460
MOSFET for the Proposed Inverter	IR640N
MOSFET used in auxiliary circuit	STW40N60M2
Switch on state resistance	0.27Ω
Body diode forward voltage drop	0.5V
Body diode on state resistance	80mΩ
Load resistor	10Ω
Load inductor	1mH

CONCLUSION

This research paper presents an innovative voltage source inverter topology that integrates a compact two-switch auxiliary circuit, resulting in a revolutionary full-range soft-switching capability. By implementing zero-voltage switching for the main switches, the proposed design minimizes switching losses and achieves near-zero voltage with a simplified control scheme. The pulse-width modulation techniques proposed ensure soft-switching throughout the entire operating range. Through simulations, the efficiency of the proposed soft-switching VSI topology is verified, demonstrating a substantial 6.63% enhancement in efficiency for a 1kW, 10kHz VSI operation

ACKNOWLEDGMENT

The author would like to thank the management of ERDA to support and publish this paper.

REFERENCES

[1] D. Shahzad, S. Pervaiz, N. A. Zaffar, and K. K. Afridi, “GaN-based high-power-density AC–DC–AC converter for single-phase transformerless online uninterruptible power supply,” *IEEE Trans. Power Electron.*,vol. 36, no. 12, pp. 13968–13984, Dec. 2021.

[2] J. Morroni and P. Shenoy, “Understanding the trade-offs and technologies to increase power density,” *TI Power, Texas Instrument. Inc., Dallas, TX,USA,* pp. 1–13, 2020.

[3] R. Faraji, L. Ding, M. Esteki, N. Mazloum, and S. A. Khajehoddin, “Soft-switched single inductor single stage multiport bidirectional power converter for hybrid energy systems,” *IEEE Trans. Power Electron.*,vol. 36, no. 10, pp. 11298–11315, Oct. 2021.

[4] R. Samani, D. S. Beyragh, and M. Pahlevani, “A new grid-connected DC/AC inverter with soft switching and low current ripple,” *IEEE Trans.Power Electron.*, vol. 34, no. 5, pp. 4480–4496, May 2019.

[5] Y. Chen and D. Xu, “Review of soft-switching topologies for single-phase photovoltaic inverters,” *IEEE Trans. Power Electron.*, vol. 37, no. 2,pp. 1926–1944, Feb. 2022.

[6] P.J. CHRZAN and M. TURZYŃSKI “Resonant DC link inverters for AC motor drive systems – critical evaluation” *BULLETIN OF THE POLISH ACADEMY OF SCIENCES TECHNICAL SCIENCES*, Vol. 67, No. 2, 2019.

[7] D. M. Divan, “The resonant DC link converter-a new concept in static power conversion,” in *IEEE Trans. Ind. Applicat.*, vol. 25, no. 2, pp. 317-325, March-April 1989.

[8] D. D. Vracar, “A Short Overview of Active-Clamped Resonant DC Link Inverter,” 2020 *Inter. Symp. on Ind. Electro. and Applicat. (INDEL)*, Banja Luka, Bosnia and Herzegovina, 2020.

[9] J. Song, E. Chu, W. Wang, L. Gao, J. Li and X. Lin, “A Resonant DC-Link Inverter and Its Voltage Compensation Strategy,” in *IEEE J. Emerg. Sel. TopicsPower Electron.*, vol. 11, no. 1, pp. 775–785, Feb. 2023

[10] S. Y. R. Hui, E. S. Gogani and Jian Zhang, “Analysis of a quasi-resonant circuit for soft-switched inverters,” in IEEE Trans. Power Electron., vol. 11, no. 1, pp. 106-114, Jan. 1996.

[11] J. Kedarisetti and P. Mutschler, “A Motor-Friendly Quasi-Resonant DC-Link Inverter With Lossless Variable Zero-Voltage Duration,” *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2613-2622, May 2012.

[12] M. Turzynski, P. J. Chrzan, M. Kolincio and S. Burkiewicz, “Quasi-resonant DC-link voltage inverter with enhanced zero-voltage switching control,” *19th Eur. Conf. Power Electron. Appl. (EPE’17 ECCE Europe)*, Warsaw, Poland,pp.P.1-P.8, 2017.

[13] S. Mandrek and P. J. Chrzan, “Quasi-Resonant DC-Link Inverter With a Reduced Number of Active Elements,” in IEEE Trans. on Industrial Electronics, vol. 54, no. 4, pp. 2088-2094, Aug. 2007.

[14] C. -M. Wang, C. -H. Su, M. -C. Jiang and Y. -C. Lin, “A ZVS-PWM Single-Phase Inverter Using a Simple ZVS-PWM Commutation Cell,” in *IEEE Trans. on Ind. Electro.*, vol. 55, no. 2, pp. 758-766, Feb. 2008.

[15] M. Hazrati-Karkaragh, M. Esteki, M. R. Mohammadi and S. A. Khajehoddin, “A Novel High-Frequency Inverter With ZVT in a Wide Range of Duty Cycles and PFs,” in *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9983-9997, Aug. 2023.

[16] E. Chu, M. Wu, L. Huang, X. Hou and H. Zhang, “Research on a Novel Modulation Strategy for Auxiliary Resonant Commutated Pole Inverter With the Smallest Loss in Auxiliary Commutation Circuits,” *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1103-1117, March 2014.

[17] M. R. Amini and H. Farzanehfard, “Three-Phase Soft-Switching Inverter With Minimum Components,” in *IEEE Trans. on Ind. Electro.*, vol. 58, no. 6, pp. 2258-2264, June 2011.

[18] H. Raee, A. Rabiei, and T. Thirnger, ”Analytical prediction of switching losses in MOSFETs for variable drain-source voltage and current applications,” in *2013 IEEE 8th Conf. on Ind. Electr. and App. (ICIEA), Australia,* 2013, pp. 705-709.

[19] D. Graovac, M. Pürschel, A. Kiep, MOSFET Power Losses Calculation Using the Data-Sheet Parameters, Infineon Application Note, 2006.

[20] K. Makrani, J.Nama, P.Modi, ”A Soft Switched Voltage Source Inverter Topology” in *IEEE confer. on pow. Electro.* Accepted 2024.