Design of a Frequency-Tunable Sinusoidal Oscillator with Grounded Capacitors and Single-Resistor Control Using One CFA

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Abstract: *This paper introduces a variable-frequency oscillator (VFO) utilizing a current feedback amplifier (CFA) with grounded capacitors. The oscillation frequency (f_0) is tunable via a single resistor, while the oscillation condition (CO) is set by a specific capacitor ratio. The circuit achieves a high-Q filter response under a nominal input (V_i), and is designed following the short-circuit natural-frequency (SCNF) approach, where the nominal input ($V_i \approx 0$) is grounded. By setting a high Q-factor ($Q \rightarrow \infty$), sustained oscillations at the pole frequency (f_0) are generated. The effects of CFA port roll-off parameters are negligible in this configuration. The design was implemented with an f_0 of approximately 9.5 MHz and phase noise of –98 dBc/Hz at a 21 kHz offset frequency, with experimental verification. An extension of the design leverages the parasitic capacitance (C_z) of the CFA to adjust f_0, eliminating the need for one discrete capacitor and expanding the frequency range up to 22 MHz.*

Keywords: SCNF, single-R tuned oscillator, CFA, variable-Q filter

I. Introduction

The design of variable-frequency sinusoidal oscillators employing a single current-feedback amplifier (CFA) as an active building block (ABB) is comparatively rare in the literature, as summarized in Table I [1-6]. A notable instance of a single-CFA fixed-frequency oscillator design was previously reported [1]. Grounded-capacitor oscillator configurations utilizing a single CFA offer distinct advantages, including enhanced immunity to device nonidealities and improved suitability for integration.One widely accessible CFA, the AD-844 [25], functions as a transresistance amplifier characterized by low distortion, high transfer-function accuracy, and a broad bandwidth, features that stem from its current-feedback architecture. Additionally, its bandwidth remains largely unaffected by changes in closed-loop gain [2,12]. In this study, we introduce a novel tunable oscillator design based on a single CFA and single resistor, using the single-capacitor negative feedback (SCNF) approach [13]—a concept that has not been extensively discussed in recent literature. Although prior works have examined [4,6] single-active-building-block (ABB) designs for filters and oscillators [3,7,14-16,20-23], the effects of device nonidealities in these designs remain largely unaddressed [27,28,30].

Table I. Comparative Study of Single-ABB Tunable Oscillators Employing a Single Resistor

Ref.	ABB	fo(Hz)-Range
1	Voltage-opamp (VOA)	1.6K
Ref.	ABB	fo(Hz)-Range
1	Voltage-opamp (VOA)	1.6K
2	CC II	1.0K
3	CFA	200K
4	OTRA	1.6K
5	CFOA	123K
6	CDTA	53.9K
proposed	CFA	22 M

II. Proposed Design

The circuit analysis in Fig. 1 is performed using the CFA-port relationships: iz=αix, vx=βvy and vo=δvz, where ideally, α=β=δ=1. Utilizing the single-capacitor negative feedback (SCNF) concept and assuming a nominal input Vi, the open-circuit transfer function is derived, incorporating device parasitic capacitances Cy and Cz.

$$H(s) = \{sR_2C_o + a + 1\} / (s^2 d_2 + s\, d_1 + d_o) \quad (1)$$
$$\text{where } d_o = 1 - b \quad (2)$$
$$d_1 = R_1C_1(1+\sigma) + R_2C_2(1+\rho) + R_1\{C_2(1+\rho) - C_o\} \quad (3)$$
$$d_2 = R_2C_2(1+\rho) + R_1C_1(1+\sigma); \sigma = C_y/C_1 < 1 \quad (4)$$

$\rho = C_z/C_2 < 1$, $a = R_2/R_o$, $b = R_1/R_o$, where $3 < C_{y,z}$ (pF) < 6 are parasitic capacitors [8] shunt parasitic resistors ($r_{y,z} > 5M\Omega$) These effects are disregarded, as all practical circuit resistors are in the kΩ range.

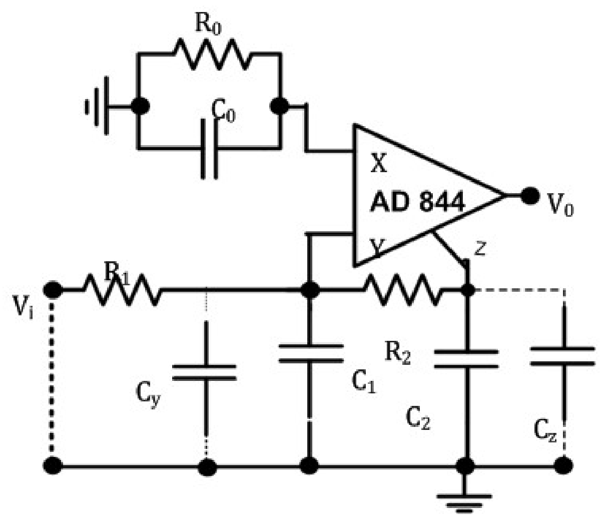


Figure1. Tunable Oscillator Design with a Single Resistor (Ro)

Based on the SCNF concept, by increasing the pole quality factor Q{=√(dod2)/d1} (where d1≈0), the circuit achieves a pair of poles on the imaginary axis. When the input V_i is then grounded (Vi≈0), the circuit produces a sustained sinusoidal oscillation at the natural pole frequency ωo = √(do/d2). Simplification with R1=R=R2, C1=C=C2, Ro=R/b and q= Co/C, yields :

$$\omega_o = \sqrt{(1-b)}/RC \quad (5)$$
$$Q = \omega_0 RC/(3 - q) \quad (6)$$

Hence, while $q \equiv Co/C = 3$ ($Q \sim \infty$) sets the condition of oscillation (CO), grounded-resistor Ro tunes fo independently.

III. Effect Of Port Rolloff

The CFA port-rolloffs may be expressed as $\alpha = (1 - \varepsilon_i)/(s\tau_i + 1)$, $\beta = (1 - \varepsilon_v)/(s\tau_v + 1)$ and $\delta = (1 - \varepsilon_0)/(s\tau_z + 1)$ where the d.c. gain errors are quite low ($\varepsilon i,v,z << 1$) ; practically the d.c. gains are all unity [8,17]. The roll-off poles occur at several hundred MHz, positioned in close proximity to each other [12]. So, we can write

$\tau_{i,v,z} = \tau_p \equiv 1/\omega_p$ and $\tau = RC$.

After re-analysis then gets modified denominator polynomial of eq.(1) as

$$D(s)= (s^2 \tau_p \tau)^2 + s^3(2 \tau^2\tau_p + 3 \tau \tau_p^2) + s^2(\tau^2 + \tau_p^2 + 6 \tau \tau_p) + s\{(3 - q) \tau + 2\tau_p\} + (1-b) \quad (7)$$

This can be simplified further in jω-domain after writing $\mu = \omega \tau p \equiv \omega/\omega p << 1$, and $\lambda = \omega RC$, given by

$$D(\omega) = [(\lambda\mu)^2 - \mu(6 \lambda + \mu) \} + (1-b) - \lambda^2] + j[\lambda(3 - q) + 2 \mu + \mu\lambda(2 \lambda + 3 \mu)] \quad (8)$$

With $\mu << 1$, eq.(8) reduces to

$$D(\omega) = \{(1-b) - \lambda^2\} + j \{\lambda(3- q)\} \quad (9)$$

By setting the real and imaginary parts to zero, the nominal design equations are obtained as shown in Eqs. (5) and (6). Here, the real part determines the oscillation frequency (ω_0), while the imaginary part provides the value for CO.

$$f_0 \approx 0.16\sqrt{(1-b)}/RC \text{ and } C_o=3C \quad (10)$$

The above derivations show that the proposed implementation remains unaffected by the roll-off poles of the CFA device, aligning closely with the ideal design equations in Eqs. (5) and (6).

IV. Parasitic Capacitor based Design

The analysis in Section 2 follows the conventional approach of disregarding the ratios between the device's parasitic capacitors (C_γ, C_z) and the adjacent grounded discrete capacitors (C_1, C_2) shown in Fig. 1. However, closer consideration suggests that including these parasitic capacitors (C_γ, C_z) in the design, as referenced in [29], could significantly expand the f_o range, allowing for the potential elimination of one discrete capacitor (C_2). Notably, the CFA's wide bandwidth can be fully leveraged when the device's pole characteristics are integrated into the circuit design [12,2,29].

Re-evaluating with R1=R=R2 produces updated coefficients for the denominator as

$$đ_2 = C_z C_1 R^2 \quad (11)$$

$$đ_1 = RC_1 \{ n + p (m+2) \} + 1 - (C_o/C_1) \quad (12)$$

$$đ_o = 2n + m + 1 - (R/R_o) \quad (13)$$

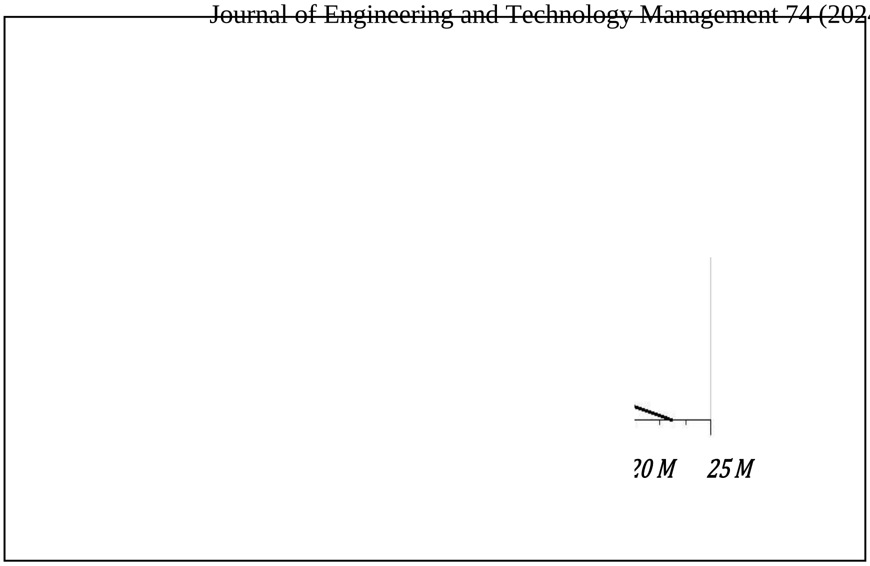
where $m=R/ry<< 1$, $n=R/rz<< 1$ and $p=Cz/C1$. Equating eq.(12) to zero, we get the CO as $C_0 = 2C_z + C_1$; then by eqs. (10) and (12) the oscillation frequency is

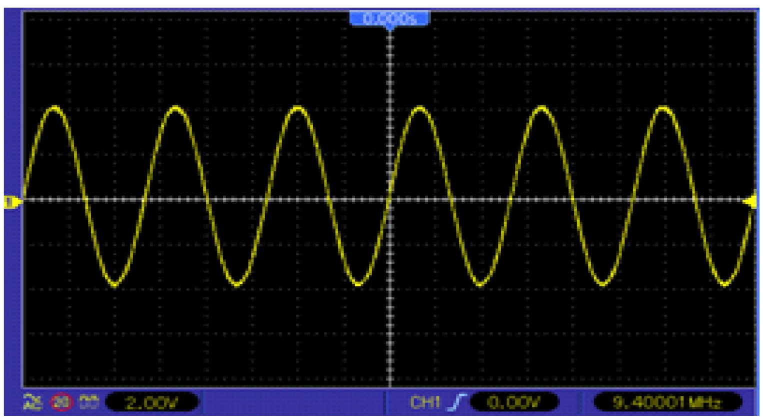
$$\omega_o = \sqrt{[(1 - b) / C_zC_1]} /R ; m, n << 1; b = R/R_o \quad (14)$$

Thus, the capability for independent adjustment of CO using C_0 and C_1, along with tuning of ω_0 via a single resistor R_0, is maintained.

V. Experimental Results

The design was practically implemented and verified through both PSPICE simulations and a hardware setup; the results are presented. in Fig.2





Theoretical
C= 40pF, C_z=6pF,R=330Ω
C= 40pF, R=330Ω

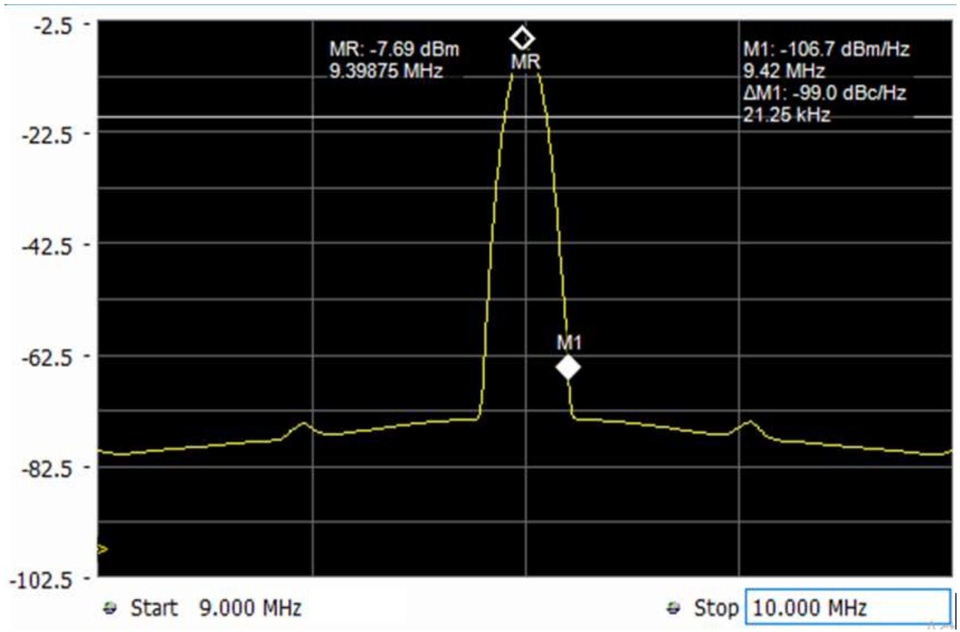


Fig. 2 .(a) Filter response with nominal-Vi designed for f_o =6.3MHz and Q = 4.5
(b) Experimentally observed sinusoid wave generation at f_o = 9.5MHz with discrete capacitors
(c) f_o- tuning characteristics
(d) Measured phase-noise Spectrum

VI. Conclusions

We propose a tunable sinusoidal oscillator that utilizes a single resistor in conjunction with a readily available AD-844 CFA element. The circuit offset (CO) and oscillation frequency (f_0) can be adjusted independently. Analysis shows that the effects of device non-idealities are minimal. An alternative design approach leverages the internal z-node capacitor (C_z) of the CFA device, allowing for the removal of one discrete capacitor and resulting in an extended fo-tunability range. The experimental results have been validated through both hardware implementation and simulation, demonstrating tunability within the frequency range of $1 \leq f_0(\text{MHz}) \leq 10$, achieved using a discrete capacitor design. A satisfactory phase noise level of ─98 dB_c/Hz was confirmed at a 21.43 kHz offset frequency when tuned to 9.5 MHz. As anticipated, this tuning range was extended to approximately fo~ 22 MHz by including C_z in the proposed design and removing C_2, while still maintaining satisfactory phase noise performance within this expanded range. Compared to recent work [9], which reports phase noise of (─)86.61 dBc/Hz phase-noise at 10KHz offset with 1.05 MHz operating frequency, the proposed design exhibits improved phase noise characteristics. Furthermore, recent studies [10] indicate growing interest in using a single, commercially available ABB for applications in signal processing and filtering.

VII. References

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