High Speed and Energy Efficient FIR Filter Implementation with Truncated Multiplier using 10T GDI Full Adder

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***Abstract*— This research investigation will use a single-bit full adder to develop a multiplier, which is a vital arithmetic operation in modern technology and will determine the outcome of the work presented in this paper. There have been several modern designs of multipliers, including the Vedic multiplier, the Wallace tree multiplier, the booth multiplier, and the approximation multiplier, all of which place a premium on the addition unit in order to reduce the arithmetic logic and improve processing performance. For this reason, the proposed work will use a truncated multiplier design. This is because a truncated multiplier can reduce the size of both the internal and external architecture of a given design by rounding, deleting, or truncating the LSB bits. In this case, the MSB bits will be truncated, and the result of an n-by-n multiplication will be presented at a single n-bit level. This proposed effort would use CMOS logic gate design to create entire adders with a 10-T transistor level and 45nm technology, demonstrating significant improvements in these metrics. The simulation results show that the proposed adder circuit employing the GDI method module reduces power consumption by 91.5%, reduces latency by 93.2%, and reduces the system's PDP by 91.64% compared to the state-of-the-art 65nm CMOS Technology. When operating at 100 KHz, Amp 0.5V, offset 2.5v, and input voltage 1.8v, the 8-order FIR filter design wastes 0.7068 nW without degrading the filter frequency response or the signal-to-noise ratio (SNR) of recorded 8-bit Modulation signals. Improved space and power savings for CMOS VLSI Filters are made possible by our approximation adder technique.**

***Index Terms*—Conventional Adder, GDI Full Adder, Hybrid Full Adder, Truncated Multiplier, FIR Filter.**

I. INTRODUCTION

Numerous research initiatives have been triggered as a result of the fast growth of portable digital applications due to the desire for ever-increasing speed, more compact implementation, and lower power consumption. The need to increase the performance of logic circuits, which were originally based on conventional CMOS technology, has resulted in the development of a wide variety of methodologies for logic design over the course of the last two decades. The widespread use of arithmetic units in contemporary integrated circuit technology causes a need for implementations of fundamental logic components that are high-performance while taking up a little amount of area. The addition operation is one of the most crucial aspects of any logic system. A number of different adder circuits have been investigated and described in the published research in an effort to reach a design that is optimum in terms of delay, power, and area [1]. In very large scale integration (VLSI), power consumption is a key factor. As power use increases, so does heat production, shortening the battery's useful life and necessitating a cooling fan to keep the electronics from overheating. Therefore, battery life and overall system cost are both impacted by power usage. Applications like digital signal processing, image processing, and microcontrollers use various arithmetic and logic operations to perform tasks like adding, subtracting, multiplying, and dividing. Internally, just adder cells were required to conduct arithmetic operations, due to the crucial role played by the one-bit adder circuit (cell) in the development of these digital communication tools. Adder cells play a crucial role in determining the overall performance of digital communication devices because of how often they are used to execute addition operations on one or more bits. As a result of the increasing complexity introduced to circuits in order to decrease the chip size, power consumption and performance of the adder circuit are suffering. Thus, in low power VLSI design, there is a focus on circuits with the goal of decreasing chip size and power dissipation. The designers of a wide array of technologies have created and used a number of effective strategies in their work. Gate-Diffusion-Input, or GDI, is a design approach that was recently created and presents an efficient alternative for logic design in mainstream CMOS and SOI technologies [2]. This technique is known as the Gate-Diffusion-Input.

This study analyzed high-performance architecture for digital signal processing applications and compared three different 1-bit Full Adder methods. Minimizing signal noise and fluctuations across all applications is a top priority in our DSP implementation, with extraordinary focus on the multiplier. To enable the sharing of arithmetic operations inside a DSP system, this method employs the use of a computing core for all arithmetic operations within a CMOS logic based architecture, with a focus on prioritizing multiplication. Therefore, the goal of improving gadget performance is to improve both speed and energy efficiency, while simultaneously reducing the device's overall size and its need for power. In digital signal processing, the FIR filter is widely used due to its ability to function at large sampling

rates, to filter in an order determined by the impulse response, and to have a precise cut-off frequency. To get the required filter output, the FIR filter design requires a certain number of adders, multipliers, and delayed components. Rounding mistakes in arithmetic operations like adding and multiplying are absent in the calculation of a FIR filter. There is no upper limit on the output values generated by the FIR filter, and it may generate an impulse response up to Nth order. Crossover filter design, mastering, seismology, and data transmission are all examples of phase-sensitive applications that may benefit from the ease with which a series of linear phase coefficients can be designed and configured. The filter's coefficients are tailored to meet time- and frequency-domain requirements. FIR filter design has a few downsides, the most significant ones being greater power consumption and the necessity for a bigger area size to house the necessary Nth-order multiplier, adders, and delayed components [3].

Inherent pipelined operations will be carried out by the MCM multiplication and normal adders included into the High-performance FIR Filter design, and the results will be generated in a way that significantly reduces the number of calculations required. Good performance across a wide frequency range necessitates a big area and strict order in the construction of the FIR Filter. The Fig.1 layout calls for the use of MCM (Multiple constant multiplication) with two input adders, and register elements. Increasing the FIR filter's Nth order improves its efficiency, but at the cost of necessitating more arithmetic and division operations. FIR filters may be efficiently implemented with the help of Distributed Arithmetic and MCM. Lookup tables are used in DA-design to save previously calculated results, reducing the need for further computation described in [4]. The amount of sums that must be performed is cut down using the MCM method. Because it takes use of reusing building blocks of code, this technique is also more productive than others. This block-based method can only be realized in transpose form, but it is well-suited to the development of high-order filters with constant coefficients.

Considering that in many digital systems, multiplication is a basic process. There are some basic proposals for multipliers shown. The hybrid-radix Booth encoding method is often used for multipliers with greater bit widths. The truncated multiplier is the primary focus of this technique because it is a hardware-efficient multiplier that can increase tradeoff accuracy while decreasing hardware cost. This is because the truncated multiplier can generate an n-bit result from an n-bit by n-bit multiplication in a relatively short amount of time by deleting, reducing, and truncating some of the partial products. In order to decrease the extra logic sizes and power consumption in truncated multiplier, this study included a 1 bit GDI Full Adder instead of the traditional full adder design. Due to its superior performance and lower hardware cost, this truncated multiplier was subsequently used into FIR filter design in place of MCM multiplication [5]. Following is a breakdown of how the remaining sections of this project are laid out. Explain the rationale for the proposed design of the GDI full adder in Section II. The functionality and efficiency of GDI Truncation are discussed in Section III. In Section IV, we discuss the 8th Order FIR Filter design's digital signal processing architecture and its performance using a Truncated Multipliers, and the study is brought to a conclusion in Section VI.

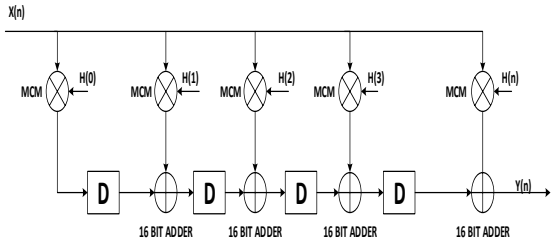

Figure 1 : Multiple Constant Multiplication based FIR Filter Design

II. Proposed GDI Full Adder Design

At first look, the GDI basic cell is similar to the normal CMOS inverter; nevertheless, there are some crucial distinctions between the two: The GDI cell has three inputs: G, P, and N. G is the common gate input of both NMOS and PMOS; P is the input to the source/drain of PMOS; and N is the input to the source/drain of NMOS. It is important to note that the ordinary p-well CMOS process is not capable of performing all of the tasks; however, the twin-well CMOS or SO1 technologies are able to effectively implement all of the functions. GDI circuit implemented in this work comprises of two XOR gates which are created by utilizing four transistors each as shown in Fig.2. The design of the Gate Diffusion Input (GDI) complete adder cell consists of two XOR/XNOR gates [6]. The GDI full adder cell only needs 10 transistors, which is a much lower number of components when compared to traditional CMOS design. Additionally, the GDI full adder cell's processing speed is higher to that of typical CMOS design.

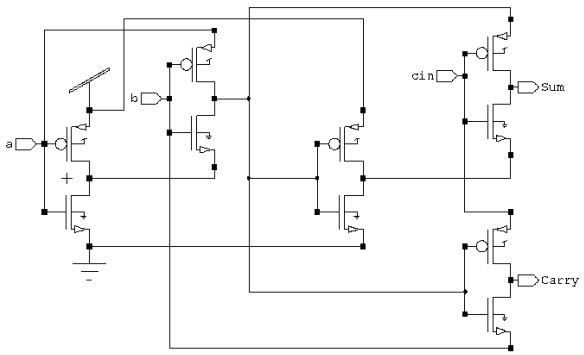

Figure 2 : 10T GDI 1-Bit Full Adder

In the present research, we examined three distinct full adder designs in order to realize our primary goal, which was to achieve high performance. The first full adder is a conventional 28T full adder, the second full adder is a hybrid 22T full adder, and the third full adder is a proposed GDI 10T full adder design. All three full adder architecture were identical in every other respect [7]. It will be presented below according to this entire adder analysis with differed voltages and different area sizes measured in nanometers (nm). The

varied average delays of these complete adders are displayed in Table.1. These delays will be analyzed with input voltages of 0.8V, 1V, and 1.4V respectively. In a comparable manner, it will be examined using CMOS technology with 45nm and 65nm dimensions. In this case, the typical full adder is shown to perform well in 1.4V. This is due to the fact that, in comparison to 0.8V and 1V, it will occupy more delay in each of the differing area sizes. When compared to this traditional full adder, the Hybrid full adder will need a lower number of transistors (22T), but in accordance with the logic of the circuit, it will occupy a longer delay in all three of its input voltages [8]. At 45 nanometers and 0.8 volts, the proposed work will have a performance time of 50.32 nanoseconds, which is a shorter delay compared to the previous two complete adders. Figure 3 displays the comparative analysis report that was conducted on the three distinct complete adders.

Table 1 : Delay Comparisons of Three Different Full Adder

	Full Adder Comparison of Average Delay at Different VDD(ns)					
	0.8 V		1 V		1.4 V	
	45nm	65nm	45nm	65nm	45nm	65nm
Conventional 28T Full Adder	100.68	101.27	100.42	100.61	99.828	99.82
Hybrid Full Adder 22T	107.45	103.39	103.51	103.91	103.86	105.20
Proposed GDI 10T Full Adder	50.32	50.45	50.58	50.64	51.86	50.79

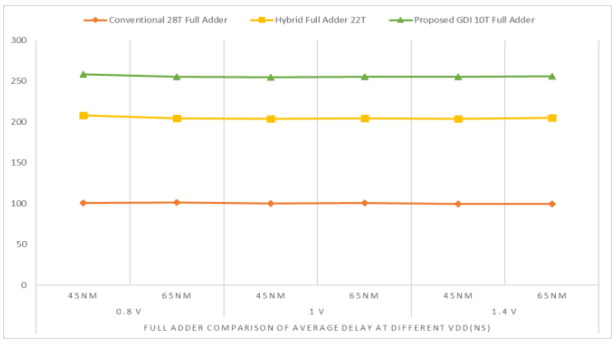

Figure 3 : Delay Comparison Analysis of Three Different Full Adder

Table 2 shows how the power output of the proposed adder and the existing adder varies depending on the Vdd (input voltage). It has been discovered that traditional 28T full adders and hybrid 22T full adder designs both provide higher power overall. At a minimal input voltage of 0.8V, the GDI full adder is capable of functioning at 0.253 W power. The architecture that has been proposed for the construction of the GDI 10T full adder would use less power. The comparative analysis report of the typical amount of power used by each of the three distinct full adders is going to be shown in Figure 4. The Tanner EDA Tool will be used to carry out this investigation. Table.3 displays the results of the Power Delay Product (PDP) study performed on three distinct full adders; the results will be compared with 0.8V, 1V, and 1.4V. Therefore, the purpose of this proposed study is to determine the proposal of a high-performance adder. The analysis of the power delay product shown in Figure 5 demonstrates the performance of a GDI 10T full adder, and it will occupy very less PDP.

Table 2 : Average Power Comparisons of Three Different Full Adder

	Full Adder Comparison of Average Power at Different VDD(µW)					
	0.8 V		1 V		1.4 V	
	45nm	65nm	45nm	65nm	45nm	65nm
Conventional 28T Full Adder	0.426	0.319	0.676	0.476	2.395	1.204
Hybrid Full Adder 22T	0.466	0.376	0.840	0.749	2.825	1.560
Proposed GDI 10T Full Adder	0.253	0.214	0.426	0.295	2.107	1.192

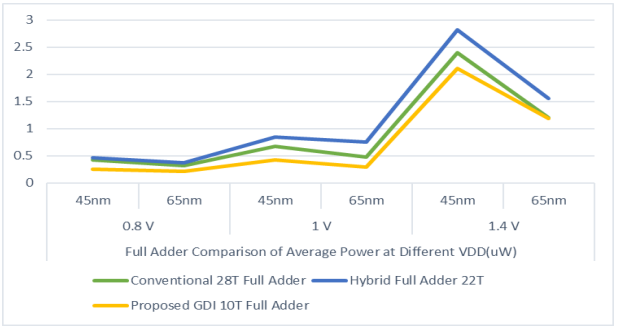

Figure 4 : Average Power Comparison Analysis of Three Different Full Adder

Table 3 : Power Delay Product of Three Different Full Adder

	Full Adder Comparison of Power Delay Product (PDP) at Different VDD					
	0.8 V		1 V		1.4 V	
	45nm	65nm	45nm	65nm	45nm	65nm
Conventional 28T Full Adder	42.93	32.299	67.907	47.93	239.12	120.28
Hybrid Full Adder 22T	50.137	38.927	86.970	77.85	293.48	164.17
Proposed GDI 10T Full Adder	12.767	10.812	21.589	14.96	109.317	60.573

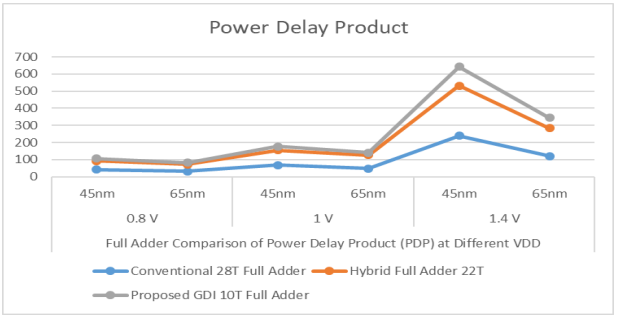

Figure 5 : Power Delay Product Comparisons of Three Different Full Adder

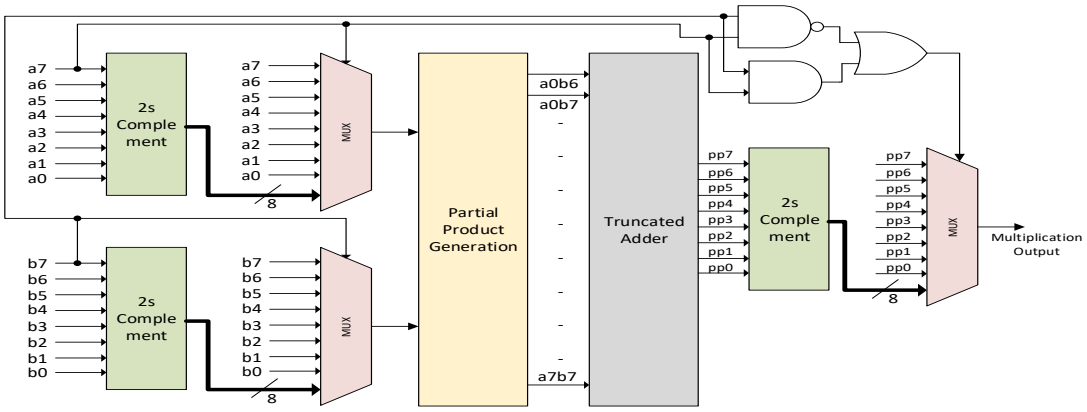

Figure 6 : Internal Architecture of Signed and Unsigned Truncated Multiplier

III. PROPOSED GDI TRUNCATED 8X8 MULTIPLIER

Using signal processing, image processing, and cryptography, this application of digital signal processing prioritizes reducing signal noise and fluctuations across all devices. These techniques are also highly valued in cutting-edge fields like 3G, LTE, Tele-Communication, audio and video processing, etc. Modern mathematical procedures will call for the use of multipliers with increased accuracy, speed, area, and power. There are three main operations involved in multiplication: producing a partial product, reducing the product, and adding the reduced product. A novel truncation multiplier is introduced in this methodological approach to multipliers [9]. This multiplier uses the truncated rounded base technique, which compares the summing output of 2n-bit partial products, this operation of 2n bits, and the LSB of rows and columns through truncation, deletion, and rounding to correction in an uneven method, in order to shrink the large area in the architecture of inner and outer architecture. A truncated multiplier that makes optimal use of logic size and space, which may be used to improving replacement accuracy while decreasing hardware costs [10]. This is due to the fact that n-bit results from n-bit multiplication may be generated in a shorter period of time appreciations to the shortened multiplier. By eliminating a larger number of columns used in the traditional method's partial product development, we save space and energy while also decreasing the wait between steps and the finished product. The lack of attention paid to carry operations (such addition and carry skip operations) and the usage of many complete adders for addition rather than the simple and efficient adder are two of the shortcomings of truncated multiplication. As can be seen in Fig. 7, truncated multipliers in this method rely entirely on regular full adders [11].

Table 4 : Comparisons of GDI 8-Bit Truncated Multiplier

	8-Bit Truncated Multiplier using GDI 10T Full Adder	
	45nm	65nm
Area(um)	121.050	174.850
Power(mw)	0.431	0.537

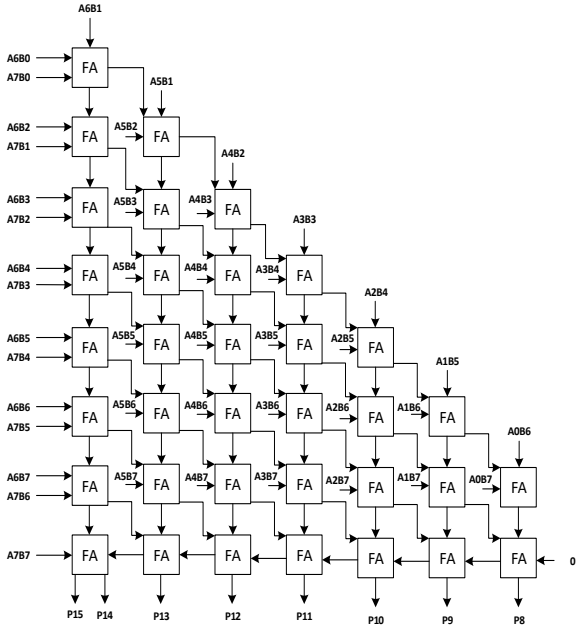

Figure 7 : Architecture of 8x8 Truncated Multiplier design

The GDI 8-bit Truncated Multiplier method that was presented was designed using Fig.2 10T GDI 1-Bit Full Adder at 45nm and 65nm CMOS Technology. In a similar fashion, the proposed approach was carried out using signed and unsigned truncated multiplier designs with the assistance of 2's complement procedures. The internal architecture of signed and unsigned truncated multipliers is shown in figure 6. It begins with the inputs a7,…a0 and b7...b0, and then it provides power to the 2s complement output, which is needed only for negative inputs. The multiplexer uses the a7 and b7 MSB sign bits to switch the output between positive and negative numbers. After the first 2s complement operation was finished [12], [13], the input data was delivered to the partial product generators. Here, we have utilized a GDI AND gate to produce a partial product, at the desired input of Fig.7's design for the truncated multiplier. Following the development of this partial product, the truncated adder begins adding with the assistance of the 10T GDI Full Adder, and its result is then provided to the 2s complement process

once again. This is done because, if we assigned a 2s complement to the input value, we then need to restore the original value by using the same 2s complement in the output [14]. In this case as well, we have switched between signed and unsigned multiplication outputs with the help of a multiplexer and an additional circuit. Table.4 displays the parameter findings of this study comparing Tanner EDA's 45nm and 65nm designs in terms of area and power consumption. Here, the 45nm size of truncated multiplier is performing well.

IV. 8TH ORDER FIR FILTER DESIGN USING PROPOSED TRUNCATED MULTIPLIER

Within the scope of digital signal processing (DSP), the process of designing digital filters is a crucial step that must be taken. Digital filters, which are fundamental building elements, are used in a variety of applications, ranging from speech processing to image processing to video processing and audio processing. FIR filters, which stand for "finite impulse response," and IIR filters, which stand for "infinite impulse response," are the two primary varieties of digital filters that are used in a wide variety of applications. Phase linearity, stability, and finite accuracy are just a few of the important traits that FIR digital filters offer over IIR filters that make them favored in a variety of situations. Adders, multipliers, and shift registers are the primary building block components that make up FIR digital filters. These components may be implemented in either hardware or software, or a mix of the two, depending on the specific circumstances. A digital filter with a finite impulse response has an impulse response that consists of a limited number of samples that are not zero. In point of fact, the FIR filter will have a finite duration of nonzero output values if it is given a nonzero input value for a finite amount of time. Non-recursive filters are whatever FIR filters are named since they don't require any output samples from the past in order to calculate the value of the current output sample [15]. FIR filters only use the current and the previous input samples. There are a lot of benefits that come along with using FIR filters, including how simple they are to comprehend and put into practice. First of all, since there is no feedback between the output and the input, these filters are always stable. This assures that the response is limited, which is a need for stability. Second, it is possible to create FIR filters with a phase that is precisely linear. Because these filters can avoid phase distortion in the signal that is transmitted through them, which may lower the system's overall performance, they are preferred in many applications (such as audio and video signal processing). In addition, FIR filters are versatile enough to be used in the implementation of a wide variety of frequency responses. The FIR filters' biggest disadvantage, on the other hand, is that, in some cases, they require more arithmetic operations, hardware components (like adders, multipliers, and delay time elements), and an enhanced filter order in order to achieve a particular level of performance [16].

The equation that describes the general equation for the implementation of the FIR filter is the discrete of a convolution formula between the input and the impulse response of the filter, which is a linear shift invariant solution given by,

$$y(n) = h(nx) * x(nx) \qquad (1)$$

$$y(n) = \sum_{k=0}^{N-1} h_k x(n-k) \qquad (2)$$

Described N[th] Order FIR Filter using (1) and (2),

$$y(n) = h_0 x(n) + h_1 x(n-1) + h_2 x(n-2) + \ldots + h_{N-1} x(n-(N-1)) \qquad (3)$$

Where the filter's input and output are represented by x(n) and y(n), respectively; the impulse response is represented by hk; the FIR filter's order is represented by N-1; and the filter has N nonzero coefficients, commonly known as the filter length. In this proposed arrangement, the architecture of the Digital FIR Filter has been altered to include a proposed GDI truncation multiplier in place of the MCM multiplier. The design appears in Figure 8. In this design, the multipliers are changed to use GDI truncated multipliers, and the adders are changed to use GDI full adders with 1 bit of precision. Based upon this filter order increases FIR Filter efficiency also increases, the output signals can be in the form of a sine wave or noise, and the filter order will have reduced the high frequency noise, with the assistance of cut-off frequency. In this proposed system, we will have designed the 8-Order of FIR Filter design [17]. Here, 1-Tap contains a single delay, single adder and single multiplier. The coefficients h (0), h (1), h (2), and h(n) will be used to determine these cut-off frequencies.

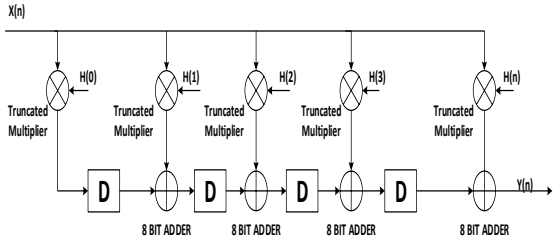

Figure 8 : FIR Filter Architecture using Truncated Multiplier

In signal processing, the use of a finite impulse response filter, also known as a FIR filter, will provide a response that is proportional to any finite length, duration, or time, and it will be produced by finding coefficients. It will match cross correlation between the input signal and the matched pulse form after the filter order has reached certain criteria based on the cut-off frequency [18]. The domain of power level will decrease, which may be the frequency domain or the time domain. In the paper, the input frequency of the FIR filter is start from 100 kilohertz, with an amplitude of 0.5 volts and an offset of 2.5 volts. The Low pass FIR Filter design is supported, and the simulation output of the filter design using Tanner EDA W-Edit is shown in Figure 9. Table.5 presents a comparison of GDI Truncated FIR Filter and Conventional Truncated FIR Filter. These filters will be generated using 45nm and 65nm CMOS technologies. In this case, the 45nm

GDI Truncated FIR filter will need less power and will occupy a smaller amount of area than its 65nm counterpart. Figure 10 displays the comparative analysis findings that were obtained from the FIR filter design [19], [20].

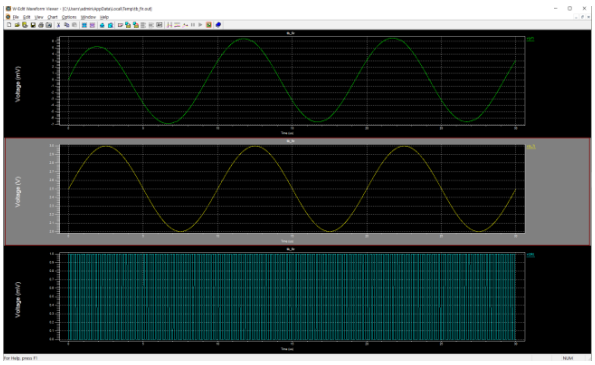

Figure 9 : W-EDIT Simulation output of FIR Filter Design

Table 5 : Comparisons of FIR Filter using GDI Truncated Multiplier

	8th Order FIR Filter using Truncated Multiplier			
	Conventional Truncation Multiplier		GDI Truncation Multiplier	
	45nm	65nm	45nm	65nm
MOSFETs	24656	24656	11632	11632
Area(um)	1109.520	1602.640	523.440	756.080
Power(nW)	3.5678	1.6790	0.7068	0.3467

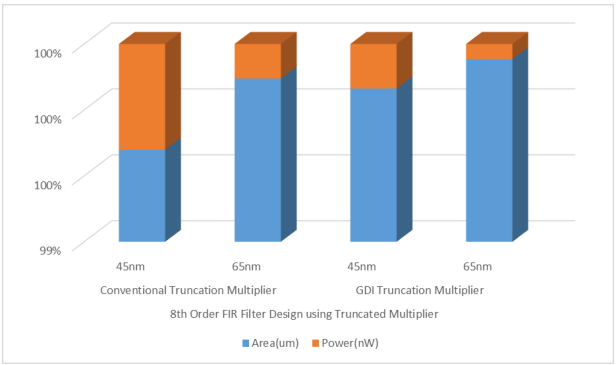

Figure 10 : Comparisons analysis of FIR Filter using Conventional and GDI Truncation Multiplier

V. CONCLUSION

The FIR Filter design implemented with Truncated Multiplier employing GDI complete adder circuits has been proposed in this article. Using the TANNER EDA tool, corresponding simulation results were created and then compared with 45nm and 65nm CMOS technology. The results of the simulation reveal that using the GDI technique module in the proposed adder circuit leads in a reduction in power consumption of 91.5%, a reduction in latency of 93.2%, and a reduction in the system's PDP of 91.64% as compared to the current state-of-the-art 65nm CMOS Technology. When compared to the conventional multiplier, the truncated multiplier demonstrates a much greater reduction in device use. The power consumption of a normal 8x8 truncated multiplier is 156 mill watts, but the power consumption of a GDI 8x8 truncated multiplier is merely 0.431 mill watts. Truncated multiplication, as proposed by GDI, is an effective way for reducing down on the amount of power dissipated as well as the area required by parallel multipliers. The design of an 8-order FIR filter that uses an operating frequency of 100 kHz, an amplitude of 0.5 volts, an offset of 2.5 volts, and an input voltage of 1.8 volts consumes 0.7068 nW of power without affecting the filter frequency response or the signal-to-noise ratio (SNR) of recorded 8-bit Modulation signals. The approximation adder method that we use enables significant improvements in terms of both space and power savings for CMOS VLSI Filters.

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